## Revision History

<table>
<thead>
<tr>
<th>Version</th>
<th>Date</th>
<th>By</th>
<th>Change Description</th>
<th>Approved</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1.0</td>
<td>2021-06-01</td>
<td></td>
<td>1:Revision preliminary version</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1.1</td>
<td>2021-06-29</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1.2</td>
<td>2021-07-24</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>V1.3</td>
<td>2021-09-13</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table of Content

01.Revision History
02.Index and Notes
03.Block Diagram
04.Power Diagram
05.Power Sequence/IO Domain Map
06.RK3568_Power/GND
07.RK3568_DDR PHY
08.RK3568_Flash/SD Controller
09.RK3568_OSC/PLL/PMUIO
10.RK3568_VO Interface_1
11.RK3568_VO Interface_2
12.RK3568_USB/PCIe/SATA PHY
13.RK3568_Audio Interface
14.RK3568_SARADC/GPIO
15.RK3568_VI Interface
16.Flash Power Manage
17.USB2/USB3 Port
18.MicroSD Card
19.SPI FLASH(Option)
20.USB HUB_FAN
21.LPDDR4X_1x32bit_200P
22.MIPI_DSI_CSI
23.eMMC Flash
24.SARADC_KEY
25.E KEY_WIFI/BT_PCIE2.0
26.HDMI
27.Ethernet
28.Headphone
29.M KEY_PCIE3.0
30.CONNECT
31.Power_CPU_RTC
32.Power_PMIC
33.Power-DC IN

Generate Bill of Materials

Header:
Item\Part\Description\PCB Footprint\Reference\Quantity\Option

Combined property string:
{Item}\{Part}\{Description}\{PCB Footprint}\{Reference}\{Quantity}\{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source, please refer to our AVL.
### Power Sequence

#### Default IO Power Domain Map

<table>
<thead>
<tr>
<th>IO Domain</th>
<th>Pin Num</th>
<th>Support IO Voltage</th>
<th>Actual assigned IO Domain Voltage</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD_NPU</td>
<td>Pin Y20</td>
<td>✓</td>
<td>VCC3V3_PMU</td>
<td>3.3V</td>
</tr>
<tr>
<td>VDDA0V9_IMAGE</td>
<td>Pin W19</td>
<td>✓</td>
<td>VCC3V3_PMU</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCCA1V8_IMAGE</td>
<td>Pin H17</td>
<td>✓</td>
<td>VCC1V8_ACODEC</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC1V8</td>
<td>Pin H18</td>
<td>✓</td>
<td>VCC1V8_ACODEC</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC3V3_SD</td>
<td>Pin L22</td>
<td>✓</td>
<td>VCC1V8_SD</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC1V8</td>
<td>Pin J21</td>
<td>✓</td>
<td>VCC1V8_SD</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC5V0_SYS</td>
<td>Pin V10</td>
<td>✓</td>
<td>VCC1V8_SD</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC3V3_SD</td>
<td>Pin V9</td>
<td>✓</td>
<td>VCC1V8_SD</td>
<td>3.3V</td>
</tr>
<tr>
<td>VCC1V8</td>
<td>Pin V12</td>
<td>✓</td>
<td>VCC1V8_SD</td>
<td>3.3V</td>
</tr>
</tbody>
</table>

If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!
RK3568_ABCDE (Power&Gnd)

Caps should be placed close to the U1000 package.

Caps should be placed under the U1000 package.

Gong Le
### RK3568_F (DDR PHY)

#### DDR4
- LPDDR4
- DDR3
- LPDDR3

<table>
<thead>
<tr>
<th>DDR4</th>
<th>LPDDR4</th>
<th>DDR3</th>
<th>LPDDR3</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPDDR4_DQS0P_B</td>
<td>LPDDR4_DQS1P_A</td>
<td>LPDDR4_DQS0N_A</td>
<td>LPDDR4_DQ14_B</td>
</tr>
<tr>
<td>LPDDR4_DQ11_B</td>
<td>LPDDR4_DQ12_A</td>
<td>LPDDR4_DQ7_B</td>
<td>LPDDR4_DQ6_B</td>
</tr>
<tr>
<td>LPDDR4_DQ6_B</td>
<td>LPDDR4_DQ3_B</td>
<td>LPDDR4_DQ1_B</td>
<td>LPDDR4_DQ9_A</td>
</tr>
<tr>
<td>LPDDR4_DQ9_A</td>
<td>LPDDR4_DM0_A</td>
<td>LPDDR4_DQ5_A</td>
<td>LPDDR4_DQ0_A</td>
</tr>
<tr>
<td>DDR3_DQS1P_B</td>
<td>DDR_DM1_B</td>
<td>DDR_DQ12_B</td>
<td>DDR_DQ9_B</td>
</tr>
<tr>
<td>DDR_DQ7_B</td>
<td>DDR_DQ6_B</td>
<td>DDR_DQ5_B</td>
<td>DDR_DQ2_B</td>
</tr>
<tr>
<td>DDR_DM1_A</td>
<td>DDR_DQ14_A</td>
<td>DDR_DQ10_A</td>
<td>DDR_DQ9_A</td>
</tr>
<tr>
<td>DDR_DQS0P_A</td>
<td>DDR_DQ6_A</td>
<td>DDR_DQ4_A</td>
<td>DDR_DQ3_A</td>
</tr>
</tbody>
</table>

For DDR4/LPDDR4/LPDDR4x mode, a 120 ohm ±1% tolerance external resistor must be connected between the DDR_RZQ pin and VDDQ pin.

For LPDDR4/LPDDR4x mode, a 120 ohm ±1% tolerance external resistor must be connected between the DDR_RZQ pin and VDDQ pin.

For DDR/LPDDR/LPDDR3 mode, a 120 ohm ±1% tolerance external resistor must be connected between the DDR_RZQ pin and VDDQ pin.

### Capacitor Placement
- Caps should be placed under the U1005 package.

### Voltage References
- VCC_DDR
- VCC_DDQ
- VCC_DQ

### Resistor Placement
- Resistors: 4.7uF, 10uF
- Capacitors: 10V, X5R

### Sheet Information
- Date: Tuesday, October 26, 2021
- Sheet Name: DDR_PHY
- Page Name: DDR_PHY
Note: If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!
RK3568_G (OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification.

PMU1 Domain
Operating Voltage=3.3V Only

PMU2 Domain
Operating Voltage=1.8V/3.3V

PMU1/2/OSC Domain Logic Power
Operating Voltage=0.9V

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.
Note: Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.
**RK3568_L(VCCIO5 Domain)**

**VCCIO5 Domain**

Operating Voltage=1.8V/3.3V

---

**Note:**
If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!

---

**Note:**
Caps of between dashed green lines and U100D should be placed under the U100D package.
Note:
In case of multiplexing, impedance control: Diff 90 Ohm ± 10%

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package.
## RK3568_H (VCCIO1 Domain)

### VCCIO1 Domain

**Operating Voltage:** 1.8V/3.3V

<table>
<thead>
<tr>
<th>Pins</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>12C1_SDA_M0 / UART3_RX_M0</td>
<td>CAN1_RX_M0</td>
</tr>
<tr>
<td></td>
<td>/ AUDIOOMUX_RXVT_P / ACODEC_ADC_DATA / GP101_A0</td>
</tr>
<tr>
<td>12C1_MCLK_M0 / UART3_RTS_M0</td>
<td>SCR_CLK / VClE3301_PER1TX_M0</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_CLK / GP101_A2</td>
</tr>
<tr>
<td>12C1_SCL_TX_M0 / UART3_CTS_M0</td>
<td>SCR_IO / VClE3301_SA0X_M0</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_M0 / GP101_A3</td>
</tr>
<tr>
<td>12C1_LBRK_TX_M0 / UART4_RTS_M0</td>
<td>SCR_RST / VClE3301.CLK0RX_M0</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_SYNC / GP101_A5</td>
</tr>
<tr>
<td>12C1_SDC0_M0 / UART4_CTS_M0</td>
<td>SCR_INT / AUDIOOMUX_BOOT_N / ACODEC_DAC_DATA / GP101_A7</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_M0 / GP101_A9</td>
</tr>
<tr>
<td>12C1_SDI0_M0 / UART4_SDI0_M0</td>
<td>/ ACODEC_DAC_M0 / GP101_B1</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_M0 / GP101_B3</td>
</tr>
<tr>
<td>12C1_SDO1_M0 / UART4_SDI1_M0</td>
<td>/ ACODEC_DAC_M0 / GP101_B5</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_M0 / GP101_B7</td>
</tr>
<tr>
<td>12C1_SDO2_M0 / UART4_SDI2_M0</td>
<td>/ ACODEC_DAC_M0 / GP101_B9</td>
</tr>
<tr>
<td></td>
<td>/ ACODEC_DAC_M0 / GP101_B11</td>
</tr>
<tr>
<td>12C1_SDI3_M0 / UART4_SDI3_M0</td>
<td>/ ACODEC_DAC_M0 / GP101_B13</td>
</tr>
</tbody>
</table>

**Default 3.3V**

---

**Note:**

If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged!

---

**Cap of between dashed green lines and U1000 should be placed under the U1000 package**

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Name: RK3568_Audio Interface

**Date:** Thursday, October 26, 2021

**Gong Le**

**Sheet:** 13 of 33
Note:
If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function.
At present, TXEN will be affected if it defaults to high level, need to add a 4.7K resistance to ground.

Note:
According to the actual choice of mounted
Cannot be mounted at the same time
Default: 1.8V
Select the voltage according to the application.

Note:
If the power domain voltage is adjusted, the software configuration must be updated synchronously, otherwise the IO may be damaged.

Note:
If there is no Key requirement, two test points must be reserved to facilitate firmware update.
It is suggested to reserve a key to facilitate the development debug.
If SARADC_VIN=0V at after power on and reset, then system will enter into loader mode.

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package. 

Note:
RK3568_K (VCCIO4 Domain)
RK3568_N (VCCIO7 Domain)
RK3568_O (SARADC/OTP)
### Flash Power Manage

<table>
<thead>
<tr>
<th>Component</th>
<th>Voltage Options</th>
<th>Flash Vol Sel State</th>
</tr>
</thead>
<tbody>
<tr>
<td>eMMC</td>
<td>1.8V</td>
<td>Logic = H</td>
</tr>
<tr>
<td>Nand flash</td>
<td>Default 3.3V, Optional 1.8V</td>
<td>Logic = L (Default)</td>
</tr>
<tr>
<td>SPI flash</td>
<td>Default 1.8V, Optional 3.3V</td>
<td>Logic = H (Default)</td>
</tr>
</tbody>
</table>

#### Note:
According to the actual choice of mounted
Cannot be mounted at the same time

---

**Diagram Note:**
- FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default.
- FLASH_VOL_SEL --&gt; Logic = H
- FLASH_VOL_SEL --&gt; Logic = L (Default)
- FLASH_VOL_SEL --&gt; Logic = H (Default)
Note: 1.8V

Default: 1.8V

If Flash is compatible, please notice when eMMC is used, the option is that @eMMC is mounted, @Nand is not mounted, @SPI Flash is not mounted. When Nand is used, the option is that @Nand is mounted, @eMMC is not mounted, @SPI Flash is not mounted. When SPI Flash is used, the option is that SPI Flash is mounted, @eMMC is not mounted, @Nand is not mounted.
Layout checked:
5V Current --> C15 --> L1 --> C14 --> C4 --> C10, finally to the pin 20 (VDD5).
**RECOVERY Key function:**
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

**Note:**
If there is no Key requirement, It is suggested to reserve a SW9200 Key to facilitate the development debug

**SARADC_VIN0_KEY/RECOVERY**
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

**PowerOn/OFF Key**
**Reset Key**

- **BOM_ID**
- **HW_ID**

---

**Title:** SARADC_KEY

**Date:** Wednesday, April 27, 2022

**Sheet:** 24 of 33
Giga PHY1

VCC_PHY0, IO Voltage Config

PHY Address Config

Note: According to the actual choice of mounted Cannot be mounted at the same time

Pull-up for additional 2ns delay to RXC for data latching

Pull-up for additional 2ns delay to TXC for data latching

Pull-up to disable PLL @ ALDP5 mode (Low power mode)

Close to PIN30

Close to PIN3, 8, 38

Close to PIN29

Close to PIN17, 40

Close to PIN14

Close to PIN42

Close to PIN9

Close to PIN10

Close to PIN11

Close to PIN12

Close to PIN13

Close to PIN14

Close to PIN15

Close to PIN16

Close to PIN17

Close to PIN18

Close to PIN19

Close to PIN20

Close to PIN21

Close to PIN22

Close to PIN23

Close to PIN24

Close to PIN25

Close to PIN26

Close to PIN27

Close to PIN28

Close to PIN29

Close to PIN30

Close to PIN31

Close to PIN32

Close to PIN33

Close to PIN34

Close to PIN35

Close to PIN36

Close to PIN37

Close to PIN38

Close to PIN39

Close to PIN40

Close to PIN41

Close to PIN42

Close to PIN43

Close to PIN44

Close to PIN45

Close to PIN46

Close to PIN47

Close to PIN48

Close to PIN49

Close to PIN50

Close to PIN51

Close to PIN52

Close to PIN53

Close to PIN54

Close to PIN55

Close to PIN56

Close to PIN57

Close to PIN58

Close to PIN59

Close to PIN60

Close to PIN61
Headphone Jack (4-pole with DET & MIC)

Option

For Headphone design, HP_SNS connect to GND near the Jack.
But, it will not support the timing poweron function. It is recommended to use external RTC IC.

Note:
The power off hold time scheme is required.