

OVERVIEW

The Raspberry Pi Compute Module (CM1), Compute Module 3 (CM3) and Compute Module 3 Lite (CM3L) are DDR2-SODIMM-mechanically-compatible System on Modules (SoMs) containing pro- cessor, memory, eMMC Flash (for CM1 and CM3) and supporting power circuitry. These modules allow a designer to leverage the Raspberry Pi hardware and software stack in their own custom systems and form factors. In addition these module have extra IO interfaces over and above what is available on the Raspberry Pi model A/B boards opening up more options for the designer.

The CM1 contains a BCM2835 processor (as used on the original Raspberry Pi and Raspberry Pi B+ models), 512MByte LPDDR2 RAM and 4Gbytes eMMC Flash. The CM3 contains a BCM2837 pro- cessor (as used on the Raspberry Pi 3), 1Gbyte LPDDR2 RAM and 4Gbytes eMMC Flash. Finally the CM3L product is the same as CM3 except the eMMC Flash is not fitted, and the SD/eMMC interface pins are available for the user to connect their own SD/eMMC device.

Note that the BCM2837 processor is an evolution of the BCM2835 processor. The only real differences are that the BCM2837 can address more RAM (up to 1Gbyte) and the ARM CPU complex has been upgraded from a single core ARM11 in BCM2835 to a Quad core Cortex A53 with dedicated 512Kbyte L2 cache in BCM2837. All IO interfaces and peripherals stay the same and hence the two chips are largely software and hardware compatible.

The pinout of CM1 and CM3 are identical. Apart from the CPU upgrade and increase in RAM the other significant hwardware differences to be aware of are that CM3 has grown from 30mm to 31mm in height, the VBAT supply can now draw significantly more power under heavy CPU load, and the HDMI HPD N 1V8 (GPIO46 1V8 on CM1) and EMMC EN N 1V8 (GPIO47 1V8 on CM1) are now driven from an IO expander rather than the processor. If a designer of a CM1 product has a suitably specified VBAT, can accomodate the extra 1mm module height increase and has followed the design rules with respect to GPIO46 1V8 and GPIO47 1V8 then a CM3 should work fine in a board designed for a CM1.



FEATURES

Hardware

- Low cost
- Low power
- High availability
- High reliability
 - Tested over millions of Raspberry Pis Produced to date
 - Module IO pins have 35u hard gold plating

Peripherals

- 48x GPIO
- 2x I2C
- 2x SPI
- 2x UART
- 2x SD/SDIO
- 1x HDMI 1.3a
- 1x USB2 HOST/OTG1x DPI (Parallel RGB Display) 1x NAND interface (SMI)
- 1x 4-lane CSI Camera Interface (up to 1Gbps per lane)
- 1x 2-lane CSI Camera Interface (up to 1Gbps per lane)
- 1x 2-lane CSI Carriera interface (up to 1Gbps per lane)
 1x 4-lane DSI Display Interface (up to 1Gbps per lane)
- 1x 2-lane DSI Display Interface (up to 1Gbps per lane)

Software

- ARMv6 (CM1) or ARMv7 (CM3, CM3L) Instruction Set
- Mature and stable Linux software stack
 - Latest Linux Kernel support
 - Many drivers upstreamed
 - Stable and well supported userland
 - Full availability of GPU functions using standard APIs



BLOCK DIAGRAM

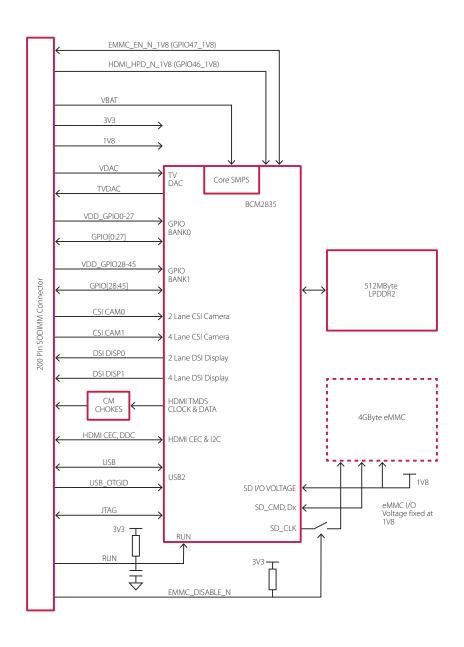


Figure 1: CM1 Block Diagram



BLOCK DIAGRAM

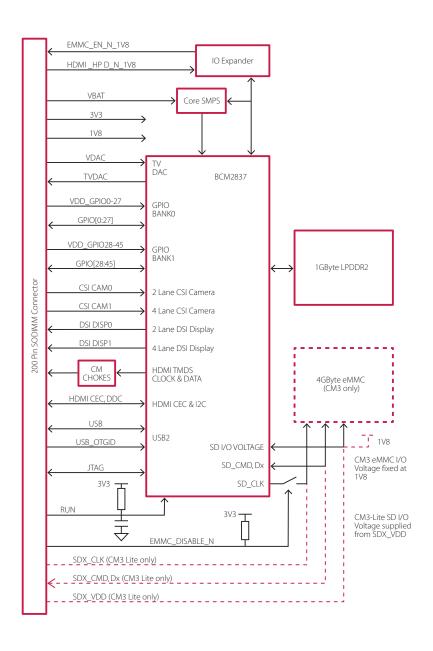


Figure 2: CM3/CM3L Block Diagram



MECHANICAL SPECIFICATION

The Compute Modules conform to JEDEC MO-224 mechanical specification for 200 pin DDR2 (1.8V) SODIMM modules (with the exception that the CM3, CM3L modules are 31mm in height rather than 30mm of CM1) and therefore should work with the many DDR2 SODIMM sockets available on the market. (Please note that the pinout of the Compute Module is not the same as a DDR2 SODIMM module; they are not electrically compatible.)

The SODIMM form factor was chosen as a way to provide the 200 pin connections using a standard, readily available and low cost connector compatible with low cost PCB manufacture.

The maximum component height on the underside of the Compute Module is 1.2mm. The maximum component height on the top side of the Compute Module is 1.5mm. The Compute Module PCB thickness is 1.0mm +/- 0.1mm.

Note that the location and arrangement of components on the Compute Module may change slightly over time due to revisions for cost and manufacturing considerations; however, maximum component heights and PCB thickness will be kept as specified.

Figure 3 gives the CM1 mechanical dimensions. Figure 4 gives the CM3 and CM3L mechanical dimensions.

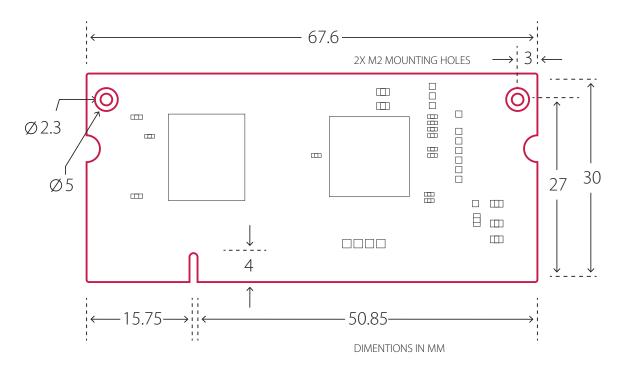


Figure 3:CM1 Mechanical Dimensions



MECHANICAL SPECIFICATION

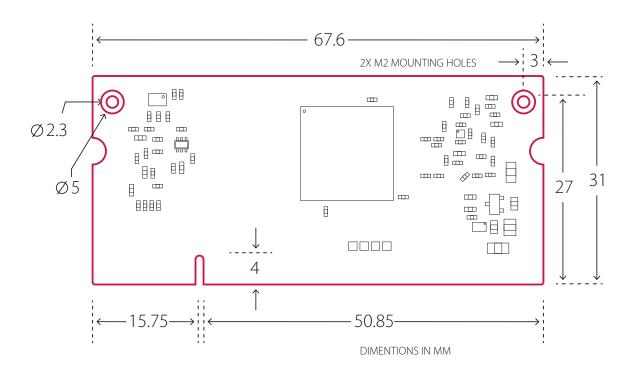


Figure 4: CM3 and CM3L Mechanical Dimension:



RASPBERRY Pi 3B+

COMPUTE MODULE 3

PIN ASSIGNMENTS

CM1 CM3 LM2 CM3 PRIL PRID CM3 CM3 CM3 CM1						
GPR00	CM1 CM3-Lite CM3	PIN		CM3	CM3-Lite	CM1
GPO1				NC		NC
GRID 7 8 CRID NC CRID NC						
GP03						
GROB						
GPD6						
GP05						
GROCK GROZY	GPIO5			NC		NC
GRIOT GRID GRID GRID GRID GRID GRID GRID GRID						
GROSS 27 2 28 GROSS 600 1 29 1 29 GROSS 600 1 1 20						
GPOS				NC		NC
GOD 331						
GRO10 33 34 GRO30 GRO31 GRO31 GRO31 GRO31 GRO31 GRO32 GRO33 GRO33 GRO32 GRO33 GRO3						
GRO11 33 8 8 GRO31 GRO22-YUDO 39 40 GRO22-YUDO GRO13 47 48 GRO22-YUDO GRO13 47 48 GRO23-YUDO GRO13 47 48 GRO33-YUDO GRO14 51 52 GRO34-YUDO GRO14 51 52 GRO34-YUDO GRO15 53 54 GRO23-YUDO GRO17 59 1 60 GRO2-YUDO GRO17 59 1 60 GRO2-YUDO GRO17 59 1 60 GRO2-YUDO GRO19 65 66 GRO33-YUDO GRO19 65 66 GRO33-YUDO GRO22 77 66 GRO23-YUDO GRO22 77 77 6 GRO24-YUDO GRO22 77 78 GRO24-YUDO GRO22 77 78 GRO24-YUDO GRO22 77 78 GRO24-YUDO GRO23 88 68 GRO33-YUDO GRO22 77 78 GRO24-YUDO GRO23 77 78 GRO24-YUDO GRO23 77 78 GRO24-YUDO GRO23 77 78 GRO24-YUDO GRO23 88 68 GRO33-YUDO GRO23 77 78 GRO24-YUDO GRO23 88 68 GRO33-YUDO GRO23 77 78 GRO24-YUDO GRO23 88 68 GRO34-YUDO GRO24 88 88 GRO34-YUDO GRO25 88 68 GRO34-YUDO GRO25 88 68 GRO34-YUDO GRO25 88 69 GRO34-YUDO GRO27 89 GRO24-YUDO GRO2						
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GPICUS 4, SUDD GNO		39				
GND	40000 17 188			_		
GP012						
GPD013						
GP014 51 52 GP034 PRO15 53 54 GP035 GR GP016 57 58 GP036 GP017 59 60 GP037 GR GP017 59 60 GP037 GR GP018 63 64 GP038 GP019 65 66 GP037 GR GP019 65 66 GP039 GP019 65 66 GP039 GP019 65 66 GP039 GP019 65 66 GP039 GP020 69 70 GP040 GP021 71 72 GP041 GP022 75 76 GP040 GP023 77 78 GP043 GP023 77 78 GP043 GP024 81 82 GP044 GP025 83 84 GP045 GP025 83 84 GP045 GP026 67 88 HDM, HPD, N, INS GP046 GP027 87 88 HDM, HPD, N, INS GP046 GP028 67 88 HDM, HPD, N, INS GP046 GP029 79 80 GS1 GP029 79 80 GS1 GP020 87 88 HDM, HPD, N, INS GP047 GP020 99 100 DS1 GP020 99 100 DS1 GS0 DS0 DS1 DS1 DS1 GS0 DS2 DS1 DS1 DS1 GS0 DS2 DS1 DS1 DS1 GS0 DS2 DS2 DS1 DS1 GS0 DS3 DS1 DS2 DS1 DS1 GS0 DS3 DS1 DS2 DS1 DS1 GS0 DS3 DS1 DS1 DS1 DS1 GS0 DS3 DS1 DS1 DS1 DS1 GS0 DS3 DS1 DS1 DS1 DS1 GS0 DS1 DS1 DS1 DS1 DS1 GS0 DS1 DS1 DS1 DS1 DS1 GS0 DS3 DS1 DS1 DS1 DS1 GS0 DS1 DS1 DS1 DS1 DS1 GS0 DS2 DS1 DS1 DS1 DS1 GS0 DS3 DS1 DS1 DS1 DS1 GS0	GPIO13	47	48		GPIO33	
PRODIS 33						
GND GP016 GP016 GP017 GP017 GP017 GP017 GP018 GR0 GP019 GP01						
GP016						
GND GPRO1S GA GPRO1S GA GPRO19 GS GND GPRO20 GND GRO20 GND GND GRO20 GND	GPIO16	57	58		GPIO36	
GPO10 65 66 GPO30 GPO40 GPO						
GPIO19 GST						
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GND	DSI0_DN1					
DSIS_DNO P9						
DSIO_DPO						
DSIO_CN	DSI0_DP0		10		DSI1_CN	
DSIO CP						
GND						
HDMI_CLE_N	DSIU_CP					
GND	GND					
HDMI_DO_P 119 120 DSII_DPI		109	11		GND	
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USB_DP 165 166 TVDAC USB_DM 167 168 USB_OTIGD GND 169 170 GND HDMI_CEC 171 172 VC_TRST_N HDMI_SDA 173 174 VC_TDI HDMI_SCL 175 176 VC_TMS RUN 177 178 V_C_TDO VDD_CORE (DO NOT CONNECT) 179 180 VC_TCC GND 181 182 GND 1V8 183 184 1V8 1V8 185 186 1V8 GND 187 188 CND VDAC 189 190 VDAC 3V3 191 192 3V3 3V3 191 192 3V3 GND 195 GND USB_TTANACTORY VDAC 189 190 VDAC 3V3 3V3 191 192 3V3 GND 197 188 GND USB_TTANACTORY GND 197 188 GND USB_TTANACTORY GND 197 188 GND USB_TTANACTORY	HDMI_CLK_N HDMI_CLK_P GND HDMI_DO_N HDMI_DO_P GND HDMI_DI_N HDMI_DI_N HDMI_DI_N HDMI_DI_N GND HDMI_DI_N HDMI_DI_N GND CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP2 CAMI_DP3	109 111 113 115 117 119 121 123 127 129 131 133 133 141 143 145 147 149 151 155 157	111 111 111 111 112 12 12 12 12 12 13 13 13 13 14 14 14 15 15 15 15		GND DSI_DP2 DSI_DN2 GND DSI_DP1 DSI_DP1 DSI_DP1 DSI_DP1 NC NC NC NC NC NC CAMO_DP0 CAMO_DP0 CAMO_CN GND CAMO_CN GN	
USB, DM 167 168 USB, OTGID GND 169 170 GND HDML CEC 171 172 VC_TRST, N HDML SDA 173 174 VC_C_TDI HDML, SCL 175 176 VC_TMS RUN 177 178 VC_TDO VDD_CORE (DO NOT CONNECT) 179 180 VC_TCK GND 181 182 GND 1VB 183 184 1V8 1V8 185 186 1V8 GND 401 187 188 GND VDACC 189 190 VDAC 3V3 191 192 3V3 3V3 193 194 3V3 GND 195 GND VDAC 197 198 GND VDAC 199 190 GND VDAC 3V3 193 194 3V3 GND 197 198 GND VDAC 199 190 GND VDAC MAT 199 199 VDAC MAT 199 199 VDAC MAT 199 199 GND VDAC MAT 199 199 VDAC	HDML CLK, N HDML CLK, P GND HDML DO, N HDML DO, P GND HDML D1, N HDML D1, N HDML D1, N HDML D1, N HDML D2, N GND CAM1, DP3 CAM1, DP3 CAM1, DP3 CAM1, DP4 CAM1, CN GND CAM1, CP CAM1, CP CAM1, CP CAM1, CP CAM1, DN1 GND CAM1, DN1 GND CAM1, DN1 GND CAM1, DN1 GND CAM1, DN1	109 111 113 115 117 119 121 125 127 129 129 131 133 135 137 139 141 143 145 147 149 151 153 155 157	111 111 111 112 12 12 12 12 12 13 13 13 13 13 14 14 14 14 15 15 15 15 15 16		GND DSI DP2 DSI DN2 GND DSI DP1 DSI DP1 DSI DP1 DSI DP1 NC NC NC NC NC NC CAMO DP0 CAMO DP0 CAMO DN0 GND CAMO	
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HDML_SDA	HDML_CLK_N HDML_CLK_P GND HDML_DD_N HDML_DD_N HDML_DD_P GND HDML_DD_N HDML_DD_N HDML_DD_N HDML_DD_N HDML_DD_N GND CAM1_DP3 CAM1_DP3 CAM1_DP2 CAM1_DP2 CAM1_DP2 CAM1_CNC GND CAM1_DP1 CAM1_DP1 CAM1_DP1 CAM1_DP0 CAM1_DP0 CAM1_DP0 CAM1_DP0 CAM1_DP0 GND	109 111 113 115 117 119 121 123 125 127 129 131 133 133 137 139 141 145 145 147 151 153 155 157 159 161 163	1111 1111 1111 1111 1111 1111 1111 1111 1111		GND DSI DP2 DSI DP2 DSI DP2 GND DSI DP1 DSI DP1 DSI DP1 DSI DP1 DSI DP1 CNC NC	
HDMI_SCL 175 176 V.C_TMS RUN 177 178 V.C_TDO VDD_CORE (DO NOT CONNECT) 179 180 V.C_TCK GND 181 182 GND 1V8 183 184 1V8 1V8 185 186 1V8 GND 187 188 GND VDAC 189 190 VDAC 3V3 191 192 3V3 GND 193 194 3V3 GND 195 196 GND VBAT 197 188 VBAT VBAT 197 189 VBAT VBAT 197 189 VBAT VAT 197 189 VBAT VAT VAT 197 189 VBAT VBAT 197 189 VBAT VC_TOK MCC_TOK MCC_TOK VC_TOK MCC_TOK MCC_TOK MCC_TOK MCC_TOK VC_TOK MCC_TOK MCC_TOK MCC_TOK MCC_TOK MCC_TOK VC_TOK MCC_TOK MCC_TOK MCC_TOK MCC_TOK MCC_TOK VC_TOK MCC_TOK	HDML CLK, N HDML CLK, P GND HDML DO, N HDML DO, P GND HDML, DO, P GND HDML, D1_N HDML, D1_N HDML, D1_N HDML D2_N HDML D2_N HDML D2_N HDML D2_P GND CAM1_DP3 CAM1_DP3 CAM1_DP3 CAM1_DP3 CAM1_DP2 CAM1_CP CAM1_CP CAM1_CP CAM1_CP CAM1_CP CAM1_CP CAM1_DP1 CAM1_D	109 111 113 115 117 119 121 123 125 127 129 131 133 135 141 147 149 149 151 153 155 157 161 163 165 167 169	111 111 111 111 111 111 111 111 111 11		GND DSI DP2 DSI DP2 DSI DN2 GND DSI DP1 DSI DP1 DSI DP1 DSI DN1 NC NC NC NC NC NC CAMO DP0 CAMO DP0 CAMO DP0 CAMO DP1 CA	
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	HDMI_CLK_N HDMI_CLK_P GND HDMI_DO_N HDMI_DO_N HDMI_DO_P GND HDMI_DI_N GND CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_DP3 CAMI_CN GND CAMI_CN GND CAMI_CP CAMI_CP CAMI_CP CAMI_CP CAMI_CP CAMI_DP1 CAMI_	109 1113 1113 1115 1117 1119 1121 1223 125 127 129 131 133 135 137 139 141 142 143 145 151 152 153 155 161 162 163 165 167 171 177 179 181 183 185 187 187 189 189 189 189 189 189 189 189	111 111 111 111 111 111 111 111 111 11		GND DSI DP2 DSI DP2 DSI DN2 GND DSI DP1 DSI DP1 DSI DP1 DSI DP1 NC NC NC NC NC NC NC NC CAMO DP1 CAMO DP0 CAMO DN0 GND CAMO DP1 CAMO DN0 CAMO DN0 GND CAMO DN0 CAMO DN1	

Table 2: Compute Module SODIMM Connector Pinout

Table 2 gives the Compute Module pinout and Table 3 gives the Compute Module pin functions.



RASPBERRY PI 3B+

COMPUTE MODULE 3

PIN ASSIGNMENTS

Pin Name	DIR	Voltage Ref	PDN ^a State	If Unused	Description/Notes
RUN and Boot Control	l (see tex	t for usage guide)			
RUN	I	3V3 ^b	Pull High	Leave open	Has internal 10k pull up
EMMC_DISABLE_N	1	3V3 ^b	Pull High	Leave open	Has internal 10k pull up
EMMC_EN_N_1V8	0	1V8	Pull High	Leave open	Has internal 2k2 pull up
GPIO					
GPIO[27:0]	I/O	GPIO0-27_VDD	Pull or Hi-Z ^c	Leave open	GPIO Bank 0
GPIO[45:28]	I/O	GPIO28-45_VDD	Pull or Hi-Z ^c	Leave open	GPIO Bank 1
Primary SD Interface ^d	e				
SDX_CLK	0	SDX_VDD	Pull High	Leave open	Primary SD interface CLK
SDX_CMD	I/O	SDX_VDD	Pull High	Leave open	Primary SD interface CMD
SDX_Dx	I/O	SDX_VDD	Pull High	Leave open	Primary SD interface DATA
USB Interface					
USB_Dx	I/O	-	Z	Leave open	Serial interface
USB_OTGID	I	3V3		Tie to GND	OTG pin detect
HDMI Interface					
HDMI_SCL	I/O	3V3 ^b	Z^{f}	Leave open	DDC Clock (5.5V tolerant)
HDMI_SDA	I/O	3V3 ^b	Z^f	Leave open	DDC Data (5.5V tolerant)
HDMI_CEC	I/O	3V3	Z	Leave open	CEC (has internal 27k pull up)
HDMI_CLKx	0	-	Z	Leave open	HDMI serial clock
HDMI_Dx	0	-	Z	Leave open	HDMI serial data
HDMI_HPD_N_1V8	I	1V8	Pull High	Leave open	HDMI hotplug detect
CAM0 (CSI0) 2-lane In	terface				
CAM0_Cx	I	-	Z	Leave open	Serial clock
CAM0_Dx	I	-	Z	Leave open	Serial data
CAM1 (CSI1) 4-lane In	terface				
CAM1_Cx	I	-	Z	Leave open	Serial clock
CAM1_Dx	I	-	Z	Leave open	Serial data
DSI0 (Display 0) 2-land	e Interfa	ce			
DSI0_Cx	0	-	Z	Leave open	Serial clock
DSI0_Dx	0	-	Z	Leave open	Serial data
DSI1 (Display 1) 4-land		ce			
DSI1_Cx	Ο	-	Z	Leave open	Serial clock
DSI1_Dx	0	-	Z	Leave open	Serial data
TV Out					
TVDAC	0	-	Z	Leave open	Composite video DAC output
JTAG Interface					
TMS	I	3V3	Z	Leave open	Has internal 50k pull up
TRST_N	I	3V3	Z	Leave open	Has internal 50k pull up
TCK	I	3V3	Z	Leave open	Has internal 50k pull up
TDI	I	3V3	Z	Leave open	Has internal 50k pull up
TDO	Ο	3V3	0	Leave open	Has internal 50k pull up

Table 3:Pin Functions

^f Requires external pull-up resistor to 5V as per HDMI spec



 $[^]a$ The PDN column indicates power-down state (when RUN pin LOW)

 $^{^{\}it b}$ Must be driven by an open-collector driver

^c GPIO have software enabled pulls which keep state over power-down

^d Only available on Lite variants

^e The CM will always try to boot from this interface first

COMPUTE MODULE 3

ELECTRICAL SPECIFICATION

Caution! Stresses above those listed in Table 4 may cause permanent damage to the device. This is a stress rating only; functional operation of the device under these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Symbol	Parameter	Minimum	Maximum	Unit
VBAT	Core SMPS Supply	-0.5	6.0	V
3V3	3V3 Supply Voltage	-0.5	4.10	٧
1V8	1V8 Supply Voltage	-0.5	2.10	٧
VDAC	TV DAC Supply	-0.5	4.10	٧
GPIO0-27_VDD	GPIO0-27 I/O Supply Voltage	-0.5	4.10	٧
GPIO28-45_VDD	GPIO28-27 I/O Supply Voltage	-0.5	4.10	٧
SDX_VDD	Primary SD/eMMC Supply Voltage	-0.5	4.10	V

Table 4: Absolute Maximum Ratings

DC Characteristics are defined in Table 5

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V _{IL}	Input low voltage ^a	VDD_IO = 1.8V VDD_IO = 2.7V	-	-	0.6 0.8	V V
VIH	Input high voltagea	VDD_IO = 1.8V VDD_IO = 2.7V	1.0 1.3	-	-	V V
I _{IL}	Input leakage current	$TA = +85^{\circ}C$	-	-	5	μΑ
C_{IN}	Input capacitance	-	-	5	-	pF
VOL	Output low voltage ^b	VDD_IO = 1.8V, IOL = -2mA VDD_IO = 2.7V, IOL = -2mA	-	-	0.2 0.15	V V
VOH	Output high voltage ^b	VDD_IO = 1.8V, IOH = 2mA VDD_IO = 2.7V, IOH = 2mA	1.6 2.5	-	-	V V
IOL	Output low current ^c	VDD_IO = 1.8V, VO = 0.4V VDD_IO = 2.7V, VO = 0.4V	12 17	-	-	mA mA
IOH	Output high current ^c	VDD_IO = 1.8V, VO = 1.4V VDD_IO = 2.7V, VO = 2.3V	10 16	-	-	mA mA
R _{PU}	Pullup resistor	-	50	-	65	$k\Omega$
R_{PD}	Pulldown resistor	-	50	-	65	$k\Omega$

Table 5: DC Characteristics



^a Hysteresis enabled

^b Default drive strength (8mA)

^c Maximum drive strength (16mA)

ELECTRICAL SPECIFICATION

AC Characteristics are defined in Table 6 and Fig. 5.

Pin Name	Symbol	Parameter	Minimum	Typical	Maximum	Unit
Digital outputs	t _{rise}	10-90% rise time ^a	-	1.6	-	ns
Digital outputs	^t fall	90-10% fall time ^a	-	1.7	-	ns
GPCLK	^t JOSC	Oscillator-derived GPCLK cycle-cycle jitter (RMS)	-	-	48	ps
GPCLK	^t JPLL	PLL-derived GPCLK cycle-cycle jitter (RMS)	-	-	20	ps

Table 6: Digital I/O Pin AC Characteristics

^a Default drive strength, CL = 5pF, VDD IOx = 3.3V



Figure 5: Digital IO Characteristics



POWER SUPPLIES

The Compute Module has six separate supplies that must be present and powered at all times; you cannot leave any of them unpowered, even if a specific interface or GPIO bank is unused. The six supplies are as follows:

- 1. VBAT is used to power the BCM283x processor core. It feeds the SMPS that generates the chip core voltage.
- **2.** 3V3 powers various BCM283x PHYs, IO and the eMMC Flash.
- **3.** 1V8 powers various BCM283x PHYs, IO and SDRAM.
- **4.** VDAC powers the composite (TV-out) DAC.
- **5.** GPIO0-27 VREF powers the GPIO 0-27 IO bank.
- **6.** GPIO28-45 VREF powers the GPIO 28-45 IO bank.

Supply	Descripion	Minimum	Typical	Maximum	Unit
VBAT	Core SMPS Supply	2.5	-	5.0+5%	V
3V3	3V3 Supply Voltage	3.3-5%	3.3	3.3+5%	V
1V8	1V8 Supply Voltage	1.8-5%	1.8	1.8+5%	V
VDAC	TV DAC Supply ^a	2.5-5%	2.8	3.3+5%	V
GPIO0-27_VDD	GPIO0-27 I/O Supply Voltage	1.8-5%	-	3.3+5%	V
GPIO28-45_VDD	GPIO28-27 I/O Supply Voltage	1.8-5%	-	3.3+5%	V
SDX_VDD	Primary SD/eMMC Supply Voltage	1.8-5%	-	3.3+5%	V

Table 7: Power Supply Operating Ranges

 $^{\it a}$ Requires a clean 2.5-2.8V supply if TV DAC is used, else connect to 3V3

Supply Sequencing

Supplies should be staggered so that the highest voltage comes up first, then the remaining voltages in descending order. This is to avoid forward biasing internal (on-chip) diodes between supplies, and causing latch-up. Alternatively supplies can be synchronised to come up at exactly the same time as long as at no point a lower voltage supply rail voltage exceeds a higher voltage supply rail voltage.



POWER SUPPLIES

Power Requirements

Exact power requirements will be heavily dependent upon the individual use case. If an on-chip subsystem is unused, it is usually in a low power state or completely turned off. For instance, if your application does not use 3D graphics then a large part of the core digital logic will never turn on and need power. This is also the case for camera and display interfaces, HDMI, USB interfaces, video encoders and decoders, and so on.

Powerchain design is critical for stable and reliable operation of the Compute Module. We strongly recommend that designers spend time measuring and verifying power requirements for their particular use case and application, as well as paying careful attention to power supply sequencing and maximum supply voltage tolerance.

Table 8 specifies the recommneded minimum power supply outputs required to power the Compute Module.

Supply	Minimum Requirement	Unit
VBAT (CM1)	2000 ^a	mW
VBAT (CM3,3L)	3500 ^a	mW
3V3	250	mA
1V8	250	mA
VDAC	25	mA
GPIO0-27_VDD	50 ^b	mA
GPIO28-45_VDD	50 ^b	mA
SDX VDD	50 ^b	mA

Table 8: Mimimum Power Supply Requirements



^a Recommended minimum. Actual power drawn is very dependent on use-case

^b Each GPIO can supply up to 16mA, aggregate current per bank must not exceed 50mA

POWER SUPPLIES

Booting

The 4GB eMMC Flash device on CM3 is directly connected to the primary BCM2837 SD/eMMC interface. These connections are not accessible on the module pins. On CM3L this SD interface is available on the SDX_pins.

When initially powered on, or after the RUN pin has been held low and then released, the BCM2837 will try to access the primary SD/eMMC interface. It will then look for a file called bootcode.bin on the primary partition (which must be FAT) to start booting the system. If it cannot access the SD/eMMC device or the boot code cannot be found, it will fall back to waiting for boot code to be written to it over USB; in other words, its USB port is in slave mode waiting to accept boot code from a suitable host.

A USB boot tool is available on Github which allows a host PC running Linux to write the BCM2837 boot code over USB to the module. That boot code then runs and provides access to the SD/eMMC as a USB mass storage device, which can then be read and written using the host PC. Note that a Raspberry Pi can be used as the host machine. For those using Windows a precompiled and packeged tool is available. For more information see here.

The Compute Module has a pin called EMMC_DISABLE_N which when shorted to GND will disable the SD/eMMC interface (by physically disconnecting the SD_CMD pin), forcing BCM2837 to boot from USB. Note that when the eMMC is disabled in this way, it takes a couple of seconds from powering up for the processor to stop attempting to talk to the SD/eMMC device and fall back to booting from USB.

Note that once booted over USB, BCM2837 needs to re-enable the SD/eMMC device (by releasing EMMC_DISABLE_N) to allow access to it as mass storage. It expects to be able to do this by driving the EMMC_EN_N 1V8 pin LOW, which at boot is initially an input with a pull up to 1V8. If an end user wishes to add the ability to access the SD/eMMC over USB in their product, similar circuitry to that used on the Compute Module IO Board to enable/disable the USB boot and SD/eMMC must be used; that is, EMMC_DISABLE_N pulled low via MOSFET(s) and released again by MOSFET, with the gate controlled by EMMC EN N 1V8. Ensure you use MOSFETs suitable for switching at 1.8V (i.e. use a device with gate threshold voltage, Vt, suitable for 1.8V switching).



PERIPHERALS

GPIO

BCM283x has in total 54 GPIO lines in 3 separate voltage banks. All GPIO pins have at least two alternative functions within the SoC. When not used for the alternate peripheral function, each GPIO pin may be set as an input (optionally as an interrupt) or an output. The alternate functions are usually peripheral I/Os, and most peripherals appear twice to allow flexibility on the choice of I/O voltage.

On CM1, CM3 and CM3L bank2 is used on the module to connect to the eMMC device and, on CM3 and CM3L, for an on-board I2C bus (to talk to the core SMPS and control the special function pins). On CM3L most of bank 2 is exposed to allow a user to connect their choice of SD card or eMMC device (if required).

Bank0 and 1 GPIOs are available for general use. GPIO0 to GPIO27 are bank 0 and GPIO28-45 make up bank1. GPIO0-27_VDD is the power supply for bank0 and GPIO28-45_VDD is the power supply for bank1. SDX_VDD is the supply for bank2 on CM3L. These supplies can be in the range 1.8V-3.3V (see Table 7) and are not optional; each bank must be powered, even when none of the GPIOs for that bank are used.

Note that the HDMI_HPD_N 1V8 and EMM_EN_N 1V8 pins (on CM1 these were called GPIO46_1V8 and GPIO47_1V8 respectively) are 1.8V IO and are used for special functions (HDMI hot plug detect and boot control respectively). Please do not use these pins for any other purpose, as the software for the Compute Module will always expect these pins to have these special functions. If they are unused please leave them unconnected.

All GPIOs except GPIO28, 29, 44 and 45 have weak in-pad pull-ups or pull-downs enabled when the device is powered on. It is recommended to add off-chip pulls to GPIO28, 29, 44 and 45 to make sure they never float during power on and initial boot.



COMPUTE MODULE 3

POWER SUPPLIES

GPIO Alternate Functions

GPIO	Default Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
0	High	SDA0	SA5	PCLK	-	-	-
1	High	SCL0	SA4	DE	-	-	-
2	High	SDA1	SA3	LCD_VSYNC	-	-	-
3	High	SCL1	SA2	LCD_HSYNC	-	-	-
4	High	GPCLK0	SA1	DPI_D0	-	-	ARM_TDI
5	High	GPCLK1	SA0	DPI_D1	-	-	ARM_TDO
6	High	GPCLK2	SOE_N	DPI_D2	-	-	ARM_RTCK
7	High	SPI0_CE1_N	SWE_N	DPI_D3	-	-	-
8	High	SPI0_CE0_N	SD0	DPI_D4	-	-	-
9	Low	SPI0_MISO	SD1	DPI_D5	-	-	-
10	Low	SPI0_MOSI	SD2	DPI_D6	-	-	-
11	Low	SPI0_SCLK	SD3	DPI_D7	-	-	-
12	Low	PWM0	SD4	DPI_D8	-	-	ARM_TMS
13	Low	PWM1	SD5	DPI_D9	-	-	ARM_TCK
14	Low	TXD0	SD6	DPI_D10	-	-	TXD1
15	Low	RXD0	SD7	DPI_D11	-	-	RXD1
16	Low	FL0	SD8	DPI_D12	CTS0	SPI1_CE2_N	CTS1
17	Low	FL1	SD9	DPI_D13	RTS0	SPI1_CE1_N	RTS1
18	Low	PCM_CLK	SD10	DPI_D14	-	SPI1_CE0_N	PWM0
19	Low	PCM_FS	SD11	DPI_D15	-	SPI1_MISO	PWM1
20	Low	PCM_DIN	SD12	DPI_D16	-	SPI1_MOSI	GPCLK0
21	Low	PCM_DOUT	SD13	DPI_D17	-	SPI1_SCLK	GPCLK1
22	Low	SD0_CLK	SD14	DPI_D18	SD1_CLK	ARM_TRST	-
23	Low	SD0_CMD	SD15	DPI_D19	SD1_CMD	ARM_RTCK	-
24	Low	SD0_DAT0	SD16	DPI_D20	SD1_DAT0	ARM_TDO	-
25	Low	SD0_DAT1	SD17	DPI_D21	SD1_DAT1	ARM_TCK	-
26	Low	SD0_DAT2	TE0	DPI_D22	SD1_DAT2	ARM_TDI	-
27	Low	SD0_DAT3	TE1	DPI_D23	SD1_DAT3	ARM_TMS	-

Table 9: GPIO Bank0 Alternate Functions



POWER SUPPLIES

GPIO Alternate Functions

GPIO	Default Pull	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5
28	None	SDA0	SA5	PCM_CLK	FL0	-	-
29	None	SCL0	SA4	PCM_FS	FL1	-	-
30	Low	TE0	SA3	PCM_DIN	CTS0	-	CTS1
31	Low	FL0	SA2	PCM_DOUT	RTS0	-	RTS1
32	Low	GPCLK0	SA1	RING_OCLK	TXD0	-	TXD1
33	Low	FL1	SA0	TE1	RXD0	-	RXD1
34	High	GPCLK0	SOE_N	TE2	SD1_CLK	-	-
35	High	SPI0_CE1_N	SWE_N	-	SD1_CMD	-	-
36	High	SPI0_CE0_N	SD0	TXD0	SD1_DAT0	-	-
37	Low	SPI0_MISO	SD1	RXD0	SD1_DAT1	-	-
38	Low	SPI0_MOSI	SD2	RTS0	SD1_DAT2	-	-
39	Low	SPI0_SCLK	SD3	CTS0	SD1_DAT3	-	-
40	Low	PWM0	SD4	-	SD1_DAT4	SPI2_MISO	TXD1
41	Low	PWM1	SD5	TE0	SD1_DAT5	SPI2_MOSI	RXD1
42	Low	GPCLK1	SD6	TE1	SD1_DAT6	SPI2_SCLK	RTS1
43	Low	GPCLK2	SD7	TE2	SD1_DAT7	SPI2_CE0_N	CTS1
44	None	GPCLK1	SDA0	SDA1	TE0	SPI2_CE1_N	-
45	None	PWM1	SCL0	SLC1	TE1	SPI2_CE2_N	-

Table 10: GPIO Bank1 Alternate Functions

Table 9 and Table 10 detail the default pin pull state and available alternate GPIO functions. Most of these alternate peripheral functions are described in detail in the Broadcom Peripherals Specification document and have Linux drivers available.



POWER SUPPLIES

Secondary Memory Interface (SMI)

The SMI peripheral is an asynchronous NAND type bus supporting Intel mode80 type transfers at 8 or 16 bit widths and available in the ALT1 positions on GPIO banks 0 and 1 (see Table 9 and Table 10). It is not publicly documented in the Broadcom Peripherals Specification but a Linux driver is available in the Raspberry Pi Github Linux repository (bcm2835_smi.c in linux/drivers/misc).

Display Parallel Interface (DPI)

A standard parallel RGB (DPI) interface is available on bank 0 GPIOs. This up-to-24-bit parallel inter-face can support a secondary display. Again this interface is not documented in the Broadcom Peripherals Specification but documentation can be found here.

SD/SDIO Interface

The BCM283x supports two SD card interfaces, SD0 and SD1.

The first (SD0) is a proprietary Broadcom controller that does not support SDIO and is the primary interface used to boot and talk to the eMMC or SDX_x signals.

The second interface (SD1) is standards compliant and can interface to SD, SDIO and eMMC devices; for example on a Raspberry Pi 3 it is used to talk to the on-board BCM43438 WiFi device in SDIO mode.

Both interfaces can support speeds up to 50MHz single ended (SD High Speed Mode).

CSI (MIPI Serial Camera)

Currently the CSI interface is not openly documented and only CSI camera sensors supported by the official Raspberry Pi firmware will work with this interface. Supported sensors are the OmniVision OV5647 and Sony IMX219.

It is recommended to attach other cameras via USB.

DSI (MIPI Serial Display)

Currently the DSI interface is not openly documented and only DSI displays supported by the official Raspberry Pi firmware will work with this interface.

Displays can also be added via the parallel DPI interface which is available as a GPIO alternate function - see Table 9 and Section 9.1.3



POWER SUPPLIES

USB

The BCM283x USB port is On-The-Go (OTG) capable. If using either as a fixed slave or fixed master, please tie the USB OTGID pin to ground.

The USB port (Pins USB_DP and USB_DM) must be routed as 90 ohm differential PCB traces.

Note that the port is capable of being used as a true OTG port however there is no official documentation. Some users have had success making this work.

HDMI

BCM283x supports HDMI V1.3a.

It is recommended that users follow a similar arrangement to the Compute Module IO Board circuitry for HDMI output.

The HDMI CK_P/N (clock) and D0-D2_P/N (data) pins must each be routed as matched length 100 ohm differential PCB traces. It is also important to make sure that each differential pair is closely phase matched. Finally, keep HDMI traces well away from other noise sources and as short as possible.

Failure to observe these design rules is likely to result in EMC failure.

Composite (TV Out)

The TVDAC pin can be used to output composite video (PAL or NTSC). Please route this signal away from noise sources and use a 75 ohm PCB trace.

Note that the TV DAC is powered from the VDAC supply which must be a clean supply of 2.5-2.8V. It is recommended users generate this supply from 3V3 using a low noise LDO.

If the TVDAC output is not used VDAC can be connected to 3V3, but it must be powered even if the TV-out functionality is unused.



POWER SUPPLIES

Thermals

The BCM283x SoC employs DVFS (Dynamic Voltage and Frequency Scaling) on the core voltage. When the processor is idle (low CPU utilisation), it will reduce the core frequency and voltage to reduce current draw and heat output. When the core utilisation exceeds a certain threshold the core votlage is increased and the core frequency is boosted to the maximum working frequency. The voltage and frequency are throttled back when the CPU load reduces back to an 'idle' level OR when the silicon temperature as mesured by the on-chip temperature sensor exceeds 85C (thermal throttling).

A designer must pay careful attention to the thermal design of products using the CM3/CM3L so that performance is not artificially curtailed due to the processor thermal throttling, as the Quad ARM complex in the BCM2837 can generate significant heat output.

Temperature Range

The operating temperature range of the module is set by the lowest maximum and highest minimum of any of the components used.

The eMMC and LPDDR2 have the narrowest range, these are rated for -25 to +80 degrees Celsius. Therefore the nominal range for the CM3 and CM3L is -25C to +80C.

However, this range is the maximum for the silicon die; therefore, users would have to take into account the heat generated when in use and make sure this does not cause the temperature to exceed 80 degrees Celsius.

Availability

Raspberry Pi guarantee availability of CM1, CM3 and CM3 Lite until at least January 2023.

Support

For support please see the hardware documentation section of the Raspberry Pi website and post questions to the Raspberry Pi forum.

