SONY

Wearable SoC with Multi-GNSS receiver and sensor engine

CXD5602GG

Description

CXD5602GG is a 32-bit RISC low power microprocessor solution for wearable applications. It is based on the ARM® Cortex® -M4F 32-bit RISC and It integrates ARM Cortex-M0+ 32-bit RISC specifically for the system controller (power management, clock, reset) and I/O processor. It incorporates embedded 1.5-Mbyte of SRAM, 64-Kbyte of backup SRAM, and 256-Kbyte of I/O processor SRAM.

The ARM Cortex-M4F and ARM Cortex-M0+ are power-gated by the Power Management Unit, respectively, that is, the CPUs are powered off by internal power switches. Processor SRAMs are able to retain data, and it's possible to restart processors quickly.

To provide optimized hardware performance for sensor fusion and audio processing services, the device integrates ultra-low power GNSS Domain, Audio Codec Domain and Sensor Domain. Sensor Domain provides the specialized engine for sensor processing.

Eliminating the need for a discrete sensor hub, these features enable various sensor applications (activity recognition, voice recognition etc.) low power audio applications such as music playback (MP3, AAC encode/decode, Bluetooth A2DP, AVRCP etc.) and hands-free communication (Bluetooth HSP, HFP).

Features

The features of CXD5602GG are:

- Application Processor
  - ARM Cortex-M4F 32-bit RISC
  - Operating frequency up to 156MHz
- 1.5M-Byte Application Memory
- Application Multi-layer Bus
  - 32-bit Multi-layer bus architecture
  - Application Domain for ARM Cortex-M4F 32-bit RISC, Audio Codec, Connectivity, Storage and Image Block
- Audio Codec
  - Class-D Amplifier (Digital Part)
  - High Resolution audio support (up to 24-bit, 192kHz)
  - Two I2S Interface support
  - Unique Audio Data Format (Pulse Density Modulation) between CXD5602GG and CXD5247GF
- 8-bit parallel Camera Interface support

- 2D Graphics Acceleration
  - BitBLT, Rotate, Scaling, Blender
- Connectivity/Storage Interface
  - On-chip USB2.0 Device support
  - eMMC 4.41 for eMMC Device
  - SD3.0 Host Controller interface
  - UART
  - SPI
  - Quad SPI-FLASH Interface
- System Control and I/O Processor (SysIOP)
  - ARM Cortex-M0+ 32-bit RISC
  - Operating frequency up to 100MHz at 1.0V
  - 256K-Byte SRAM
  - 128K-Byte ROM for secure booting
- SysIOP Domain multi-layer bus
  - 32-bit Multi-layer bus architecture
  - SysIOP Domain for ARM Cortex-M0+ 32-bit RISC, PMU, GNSS, Sensor engine, HostIF, Configurable IO
- Power management
  - I2C and GPIO interface connections to PMIC (CXD5247GF)
  - power on reset
  - power gate control
- Clock and Reset management
  - XTAL, RTC, RCOSC, PLL
- 64K-Byte Backup SRAM
- Timers
  - RTC
  - A general-purpose 32-bit timer each Processor Unit
- Host Interface
  - I2C, SPI or UART interface
  - 1K-Byte Host communication Memory
- Sensor engine
  - SPI and two I2Cs Interface
  - 40K-Byte Sensory Data FIFO
  - Pre-processing unit for sensor fusion
  - Up to Four PWMs
- ADCs
  - 4 channels 10-bit low power ADC
  - 2 channels 10-bit high performance ADC

- Multi-GNSS receiver
  - GPS (L1 C/A)
  - GLONASS (L1OF)
- Configurable I/O
  - I2C/SPI/GPIO Interfaces
- Debug
  - Serial wire debug (SWD), Embedded Trace Macrocell
  - UART support

Contents

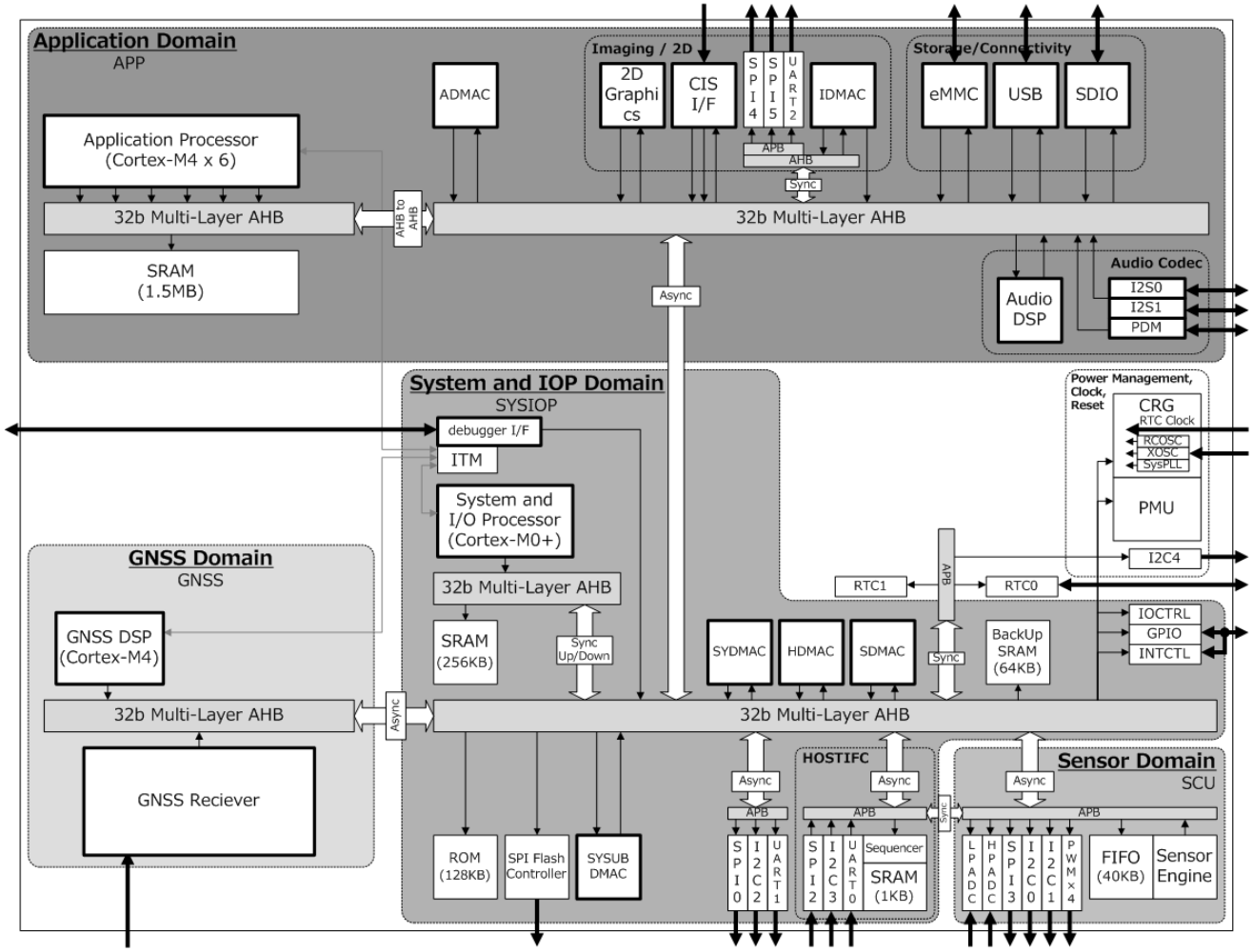
Package

CXD5602GG: MFC VFBGA (FCBGA) 185pin

Structure

Silicon-Gate CMOS

Block Diagram



Description of Functions

Application Domain

Application Processor

The application processor integrates six Cortex-M4s to meet the requirements of wearable devices, which demand operation in low power and performance-optimized consumer applications with the ability to scale in speed up to 156.0 MHz, the ARM Cortex-M4 Processor.

The key features include:

- ARM Cortex-M4 processor
  - ISA Support: Thumb/Thumb-2 technology
  - DSP Extension: Single cycle 16/32-bit MAC, Single cycle dual 16-bit MAC, 8/16-bit SIMD arithmetic, Hardware Divide (2-12 Cycles)
  - Floating Point Unit: Single precision floating point unit, IEEE 754 compliant
- Processor system peripherals
  - Programmable Interrupts Controller
    - ✧ 128 channel peripheral Interrupt support for each processors
  - Timers
    - ✧ AMBA® Design Kit (ADK) SP804
    - ✧ 2-channel support
    - ✧ One Timer module for each processor (Total: 6 Timers)
  - Watch Dog Timer
    - ✧ AMBA® Design Kit (ADK) SP805
    - ✧ One channel for each processor (Total: 6 Watch Dog Timer)

Embedded application Memory

The key features include:

- 1.5M Byte SRAM
- operating frequency
  - High Performance mode: Up to 156.0MHz
  - Low Power mode: Up to 32.736MHz

Image and Display Processing Domain

The key features Domain include:

- 8-bit parallel Camera Interface input
  - 8-bit ITU-R BT 601 / 656 Mode
  - compressed data like JPEG support
  - supports Y/C, JPEG and JPEG+Y/C Interleave formats
  - Programmable polarity of video sync signal
  - Capture frame control support
  - Input image size

- ✧ JPEG Only : up to 5M pixels
- ✧ Y/C Only : up to 480x360
- ✧ JPEG+Y/C : 2M + WQVGA (JPEG High Quality mode)
  5M + WQVGA (JPEG Normal Quality mode)

– Parallel Input rate : up to 54MHz

- SPI Interface(SPI4)
  – ARM PrimeCell Synchronous Serial Port (PL022)
  – Communication at speeds
    ✧ High Performance mode:
      - Master Half duplex mode: up to 39 Mbit/s (transmit only)
      - Master Full duplex mode: up to 9.75 Mbit/s
    ✧ Low Power mode:
      - Master Half duplex mode: up to 9.75 Mbit/s (transmit only)
      - Master Full duplex mode: up to 6.5 Mbit/s

- 2D Graphics accelerator
  – Bit Block Transfer
  – Rotator
    ✧ Supported image format: YCbCr422, RGB565
    ✧ Supported rotate degree: 0, 90, 180, 270 degrees
    ✧ Color space Conversion (YCbCr422<->RGB565)
  – 3-operand raster operation (ROP3)
  – Alpha blending
  – Scaling
    ✧ Horizontal direction: x1/64 to x64, Vertical direction: x1/64 to x64
    Maximum source input 2880x2160, maximum destination output 768x1024
    ✧ YCbCr 422 16 bpp format

Connectivity and Storage Domain

The key features are:

- USB 2.0 Device
  – Complies with USB 2.0 Specification High-speed up to 480 Mbps
    ✧ Not supported at Low Power mode:
  – On-chip USB PHY transceiver
  – Supports MSC, MTP, CDC,PTP, ACM, and HID class
  – Multi-function
    ✧ Interface: #0/#1/#2
- SD Host Controller Interface
  – SD Memory Card Protocol version 3.0 compatible

- 8K-Byte(32bit x 512word) x2 FIFOs for Tx/Rx
- Communication speeds
  - ✧ High Performance mode: up to 39.000MHz
  - ✧ Low Power mode: up to 24.552MHz

- eMMC Interface
  - eMMC 4.41 Protocol compatible
    - ✧ only SDR mode
  - 1K-Byte(32bit x 256word) x2 FIFOs for Tx/Rx
  - Communication speeds
    - ✧ High Performance mode: up to 39.000MHz
    - ✧ Low Power mode: up to 24.552MHz
- UART interfaces(UART2) :
  - PrimeCell® UART (PL011)
  - Communication speeds
    - ✧ High Performance mode: up to 3 Mbit/s
    - ✧ Low Power mode: up to 2 Mbit/s
- SPI interfaces(SPI5)
  - ARM PrimeCell Synchronous Serial Port (PL022)
  - Communication at speeds
    - ✧ High Performance mode:
      - up to 13.64 Mbit/s
    - ✧ Low Power mode:
      - up to 8.184 Mbit/s

DMAC

- A-DMAC (PL081) supports for memory to memory
- I-DMAC (like PL080) supports for SPI and UART
-

Audio Codec Domain

The key features are:

- I2S Bus Interface supports:
  - Two I2S-bus for audio-codec interface with DMA-based operation
  - 16/24-bit per channel data transfers
  - I2S, Left-justified data format
  - Various bit clock frequency and codec clock frequency support
    - ✧ Master clock:
      - High performance mode: 256fs,128fs,64fs of bit clock frequency
      - Low power mode: 128fs, 64fs of bit clock frequency
    - ✧ Slave clock:
      - High performance mode: 256fs,128fs,64fs of bit clock frequency

- Low power mode: 128fs, 64fs of bit clock frequency
- ✧ Sampling rate
  - High performance mode
    - Master mode : 192kHz, 96kHz, 48kHz
    - Slave mode: 192kHz, 96kHz, 48kHz, 44.1kHz, 16kHz, 8kHz
  - Low power mode
    - ➢ Master mode : 96kHz, 48kHz
    - ➢ Slave mode: 96kHz, 48kHz, 44.1kHz, 16kHz, 8kHz
- ✧ 2ch channels each I2S interface

- Unique Audio Data Format (Pulse Density Modulation) between CXD5602GG and CXD5247GF

Clock, Reset and Power management Domain

The key features are:

- Reset
  - Power on Reset from PMIC (CXD5247GF)
  - Power on reset in RCOSC block
  - Reset Caused by Watch Dog Timer
- RCOSC
  - 8.192MHz
  - Embedded Ring OSC
  - Calibration by using RTC(32.768 kHz)
- XOSC
  - XTAL: 26MHz
  - Supply clock to RF-PLL and SysPLL
- Real Time Clock (RTC)
  - Full clock features: sec, min, hour, date, day, month, and year
    - ✧ PreCounter (15-bit)
    - ✧ PostCounter (32-bit)
  - 32.768 kHz operation
- Sys-PLL
  - Lower power PLL on-chip System PLL which generates digital part.
- RF-PLL
  - 196.416MHz
  - PLL on-chip RF PLL which generates GNSS reference frequencies
- Watch Dog Timer (WDT)
  - Reset requirement to external device at time out via I2C bus or GPIO
- Backup SRAM
  - 64K-Byte SRAM
- ALIVE Connectivity to PMIC
  - I2C bus interface

- ✧ Standard-mode (100kbps)
- ✧ Fast-mode (400kbps)

– GPIO
- ✧ Up to 50-bit

- Power Management
  – Clock-gating control and power gating control for components
  – Various low power modes are available such as Power Off, Deep Sleep, Sleep and Standby modes
  – Power supply voltage (VDD) for Digital and SRAM Mode:
    - ✧ High Performance mode: VDD = 1.0V
    - ✧ Low Power mode: VDD = 0.7V
  – Power Domain
    - ✧ PWD_PMU
      - All components of VDD supplied logic, SRAM, ROM and analog
      - Including Clock, reset and Power management Domain and Backup SRAM and XOSC, SYSPLL
      - ALIVE GPIO
    - ✧ PWD_APP
      - All components of Application Domain
      - Including 1.5M-Byte SRAM in Application memory and Application Multi-layer Bus
    - ✧ PWD_APP_DSP
      - Application processors and DSPs block
      - A-DMAC
    - ✧ PWD_APP_SUB
      - Connectivity, Storage I/F and Camera, Display Interface in Application Domain
    - ✧ PWD_APP_AUD
      - Audio Codec
    - ✧ PWD_SCU
      - Components of sensor engine
      - Including LP-ADC,HP-ADC
    - ✧ PWD_CORE
      - All components of SYSIOP Domain and GNSS Domain
      - Including 256K-Byte SRAM in System Control and I/O Processor Memory
      - Including 640K-Byte SRAM in GNSS Memory
      - Including ALIVE I/O (I2C, GPIO)
      - Including GNSS-RF
      - ALIVE I2C
    - ✧ PWD_SYSIOP
      - System Control and I/O Domain
      - Excluding 256K-Byte SRAM in System Control and I/O Processor Memory

- ✧ PWD_SYSIOP_SUB
  - Configurable I/O (I2C,SPI,UART) Interface
  - SPI-FLASH Interface
  - 128K-Byte ROM in System Control and I/O Processor Memory
  - SYSUB-DMAC
- ✧ PWD_GNSS
  - Components of GNSS Domain
  - Excluding RF and 640K-Byte SRAM in GNSS Memory
- ✧ PWD_GNSS_ITP
  - ITP Block in GNSS Domain

– Digital I/O Domain: CXD5602GG has two I/O domain for digital block
- ✧ HOSTIF I/O Domain
- ✧ Others

System and I/O Processor Domain

System Control and I/O Processor

The I/O processor integrates one Cortex-M0+ to meet the requirements of wearable devices, which demand operation in low power and performance-optimized consumer applications with the ability to scale in speed from 32 MHz to 100 MHz, the ARM Cortex-M0+ Processor

The key features are:

- ARM Cortex-M0+ processor
  – ISA Support: Thumb Thumb-2 subset
- System Control and I/O Processor Memory
  – ROM: 128K-Byte
  – SRAM: 256K-Byte
- Boot Modes
  – It is used to download the program to either SPI-Flash memory or eMMC via one of the available interfaces (USB device, Configurable I/O<UART>, or the Host Interface<SPI, UART, and I2C>).
- Processor system peripherals
  – Inter-processor communication unit
    - ✧ communication FIFO (Tx,Rx) support
    - ✧ 16 binary semaphores support
  – Programmable Interrupts Controller
    - ✧ One channel software Generated Interrupt for each processors
    - ✧ 128 channel shared peripheral Interrupts for the application processors
  – Timers
    - ✧ AMBA® Design Kit (ADK) SP804
    - ✧ 2 channel support
  – Watch Dog Timer

- ✧ AMBA® Design Kit (ADK) SP805
- ✧ One channel support for each application processors

System Peripherals

The key features of system peripheral are:

- DMAC
  - SY-DMAC (PL081) for memory to memory transfer
  - SYSUB-DMAC(PL081) for SPI-FLASH Interface and Configurable I/O
  - S-DMAC(PL230) for Sensor Engine
  - H-DMAC(PL081) for Host Interface
- Configurable I/O (I2C,SPI,UART) Interface
  - SPI Interface(SPI0)
    - ✧ PrimeCell® SSP (PL022)
    - ✧ Master mode only,
    - ✧ Half-duplex operation only
    - ✧ Up to 8.1Mbps
  - I2C Bus Interfaces(I2C2):
    - ✧ Multimaster mode only
    - ✧ Standard-mode (100 kbps)
    - ✧ Fast-mode (400 kbps)
  - UART(UART1)
    - ✧ PrimeCell® UART (PL011)
    - ✧ Up to 2Mbps

Storage Interface

The key features are:

- Quad SPI-FLASH Interface(SPI1)
  - Quad SPI Flash Interface with 1bit or 4-bit data
  - High Performance mode: Up to 39.000MHz
  - Low Power mode: Up to 32MHz

Sensor Domain

The key features are:

- Reduced power consumption mode
  - Keep CPUs asleep
- Sensor signal processing
  - Signed data to/from unsigned data conversion
  - Gain and offset each element of vector to transform values
  - Decimation
    - ✧ Two Stage Decimating CIC Filter
    - ✧ Decimation Mode: 1/2, 1/2^2, 1/2^3

- Two dimension Infinite impulse response (IIR) filter
- Norm (Fast Approximate Distance Functions):
- Threshold decision for norm data
  - ✧ Generating interrupt cause

- Time-stamp
  - Generating time-stamp based-on RTC in PMU to add to sensory data
- Sensory Data FIFO
  - 40K-Byte with 27 partitions

    Decimation data FIFO: 2

    External sensor data FIFO: 8

    Virtual sensor data FIFO: 10

    Host-CPU communication buffer: 1
- SPI Interface(SPI3)
  - PrimeCell® SSP (PL022)
  - Master mode only
  - 3 slave select
  - Up to 6.5Mbps
- Two I2C Bus Interfaces(I2C0, I2C1)
  - Multimaster mode only
  - Standard-mode(100 kbps)
  - Fast-mode(400 kbps)
- PWM

PWM counter trigger timing can be connected to the ADC input clock to allow the application to synchronize PWM and A/D conversion.

  - Up to Four PWMs
  - Application: vibrator, beeper, LED
- A/D Conversions
  - 10-bit Low Power (LP)ADC
    - ✧ Up to 4 external channels
    - ✧ 4 channels multiplexed mode sampling rate: 256Hz
    - ✧ 1 channel mode sampling rate: 32kHz
    - ✧ Application: temperature, etc.
  - Two 10-bit High Performance (HP) ADCs
    - ✧ Up to 2MHz
    - ✧ Post decimation filter: Up to 32kHz
    - ✧ Application: vibrator, voice, etc.

Host Interface

The key features:

- UART Interface(UART0)

- PrimeCell® UART (PL011)
- High Performance mode: Up to 3Mbps
- Low Power mode: Up to 2Mbps

- SPI Interface(SPI2)
  - PrimeCell® SSP (PL022)
  - Slave mode only
  - High Performance mode: Up to 4Mbps
  - Low Power mode: Up to 2.7Mbps
- I2C Bus Interface(I2C3)
  - Slave mode only
  - Standard-mode(100 kbps)
  - Fast-mode(400 kbps)
  - Fast-mode plus (1Mbps)
- I2C3, SPI2 and UART0 interfaces are multiplexed, so that one interface is available at a time.
  - STRAP PIN: SYSTEM0, SYSTEM1

SYSTEM1	SYSTEM0	Host Interface
0	0	I2C3
0	1	UART0
1	0	SPI2
1	1	reserved

- Host Communication Memory supports
  - 1K-Byte SRAM
- Direct communication path to Sensor engine:

Bypassing the embedded Processor and let it stay asleep, which results in saving power, a faster response to external host CPU.

GNSS Domain

Multi-GNSS receiver

The features are:

- Multiple Constellation compatibility
  - GPS (L1 C/A)
  - GLONASS (L1OF)

- Position Accuracy

Item	GPS	GPS & GLONASS	Unit	Remark
2DRMS	2.5	2.5	m	Signal strength is -130 dBm Test circuit as shown in the figure below

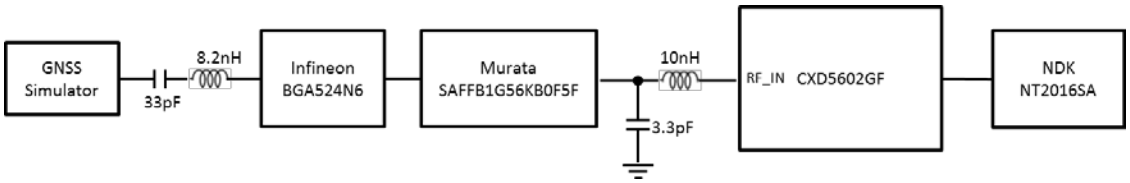
- Time-To-First-Fix (TTFF)

Item	GPS	GPS & GLONASS	Unit	Remark
Cold Start	35	35	s	Signal strength is -130 dBm Test circuit as shown in the figure below
Hot Start	2	2	s	

- Sensitivity

Item	GPS	GPS & GLONASS	Unit	Remark
Cold Start	-147	-147	dBm	Test circuit as shown in the figure below
Hot Start	-160	-160	dBm	
Tracking	-161	-161	dBm	

- Test Circuit



- Noise Filter

An embedded noise filter for GNSS signals. It is automatically enabled at the optimum settings for the input noise.

- RF Performance

Item	Min.	Typ.	Max.	Unit
Total NF	-	3	-	db

Description of Operation

Recommended operating conditions

Pin Name	Parameter		Minimum	Typical	Maximum	Unit
VDD_CORE	DC Supply Voltage for Core Block		0.65	-	1.1	V
		LP	0.65	0.7	0.75	V
		HP	0.90	1.0	1.1	V
VDD_IO_DIG	DC Supply Voltage for Digital I/O		1.65	1.8	1.95	V
VDDA_IO_ANA	DC Supply Voltage for Analog I/O		1.65	1.8	1.95	V
VDDA_IO_SENS						
VDDA_LNA	DC Supply Voltage for LNA		0.65	0.7	0.75	V
VDDA_LO	DC Supply Voltage for LO		0.65	0.7	0.75	V
VDDA_ANA_M	DC Supply Voltage for Analog		0.65	0.7	0.75	V
VDDA_SYSPLL_M						
VDDA_XOSC	DC Supply Voltage for XOSC		0.65	0.7	0.75	V
VDDA_LPADC	DC Supply Voltage for LP-ADC		0.65	0.7	0.75	V
VDDA_HPADC_M	DC Supply Voltage for HP-ADC and RCOSC		0.65	0.7	0.75	V
VDDA_USB33	DC Supply Voltage for USB		3.13	3.3	3.46	V
VDDA_USB18_M	DC Supply Voltage for USB		1.71	1.8	1.89	V
VDDA_USB10_M	DC Supply Voltage for USB		0.95	1.0	1.05	V

Absolute Maximum Ratings

Parameter	Power supply system	Symbol	Minimum	Maximum	Unit
DC Supply Voltage	0.7V	VDD07	-0.3	1.05	V
	1.0V	VDD10	-0.3	1.5	V
	1.8V	VDD18	-0.3	2.5	V
	3.3V(VDDA_USB33)	VDD33	-0.3	4.95	V
DC Input Voltage	0.7V	VIN07	-0.3	1.05	V
	1.8V	VIN18	-0.3	2.5	V
	3.3V(USB_DP/DM)	VIN33	-0.3	5.25	V

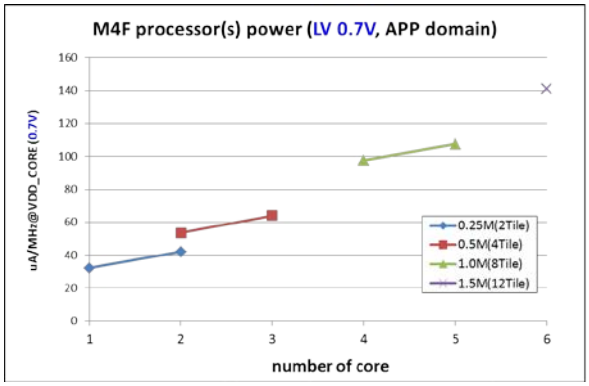
Temperature Condition

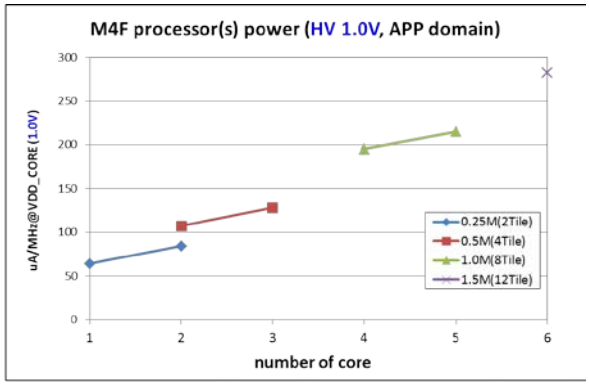
Parameter	Symbol	Range	Unit
Operating Temperature	Ta	-25 to +85	degree
Storage Temperature	Tstg	-40 to +125	degree

Power Consumption

- SysIOP Domain (including Cortex M0+) Active Power Performance
  - Low Power mode: VDD = 0.7V
    - ✧ 26 uA/MHz
  - High Performance mode: VDD = 1.0V
    - ✧ 51 uA/MHz

- Application Domain Active Power Performance
  - Low Power mode: VDD = 0.7V
    - ✧ Six Cortex-M4Fs active
      - 200 uA/MHz i.e., 34 uA/MHz,1Core
    - ✧ One Cortex-M4F active
      - 45 uA/MHz
  - High Performance mode: VDD = 1.0V
    - ✧ Six Cortex-M4Fs active
      - 282uA/MHz i.e., 48uA/MHz,1Core
    - ✧ One Cortex-M4F active
      - 64uA/MHz





Clocks

- XOSC_IN (in buffer mode)

Item	Symbol	Min.	Typ.	Max.	Unit
Input voltage range	V_{IN}	0.8	-	1.4	Vpp
Input Frequency	F_{IN}	-	26.0	-	MHz
Input frequency characteristics	F_{IN_C}	-0.5	-	0.5	ppm
Duty Cycle	D_C	40	-	60	%

- RTC_CLK_IN

Item	Symbol	Min.	Typ.	Max.	Unit
Input Frequency	F_{IN}	-	32.768	-	kHz
Frequency Tolerance	F_{IN_T}	-300	-	300	ppm
Duty Cycle	D_C	5	-	95	%

Electrical Characteristics

DC Characteristics

LVCMOS18 I/F (1.8V)

Item	Symbol	Conditions	Min	Typ.	Max	Unit
Input low level voltage	VIL		-0.3		0.35 * VDD18	V
Input high level voltage	VIH		0.65 * VDD18		VDD18 + 0.3	V
Output low level voltage	VOL	IOL= 2/4mA			0.4	V
Output high level voltage	VOH	IOH= 2/4mA	VDD18 - 0.4			V
Schmitt input hysteresis voltage	Vh		150			mV
Low level input current	IIL	Vin= VSS				
High level input current	IIH	Vin= VDD18				
PU resistance	Rpu	Vpad ‡ =0		50		kohm
PD resistance	Rpd	Vpad= VDD18		50		kohm

† VDD18: I/O Supply Voltage

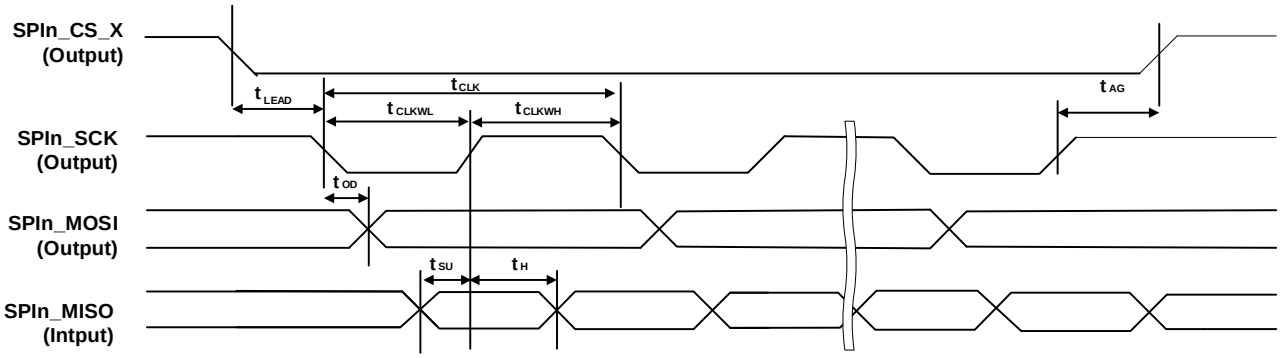
‡ Maximum allowed signal voltage level IO PAD

Digital Signal AC Characteristics

Serial peripheral interface (SPI)

The device supports up to five serial peripheral interfaces (SPI0, SPI2, SPI3, SPI4 and SPI5).

Master Mode



SPI0

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL=30pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	t_{CLK}/2-10	-	-	ns	
Chip Select Hold Time	t_{AG}	t_{CLK}-10			ns	
SCK Cycle	t_{CLK}	102.6	-	-	ns	
SCK Pulse Width-High	t_{CLKWH}	46.17	-	-	ns	
SCK Pulse Width-Low	t_{CLKWL}	46.17	-	-	ns	
Data Output Delay Time	t_{OD}	-10.0	-	10.0	ns	
Data Input Setup Time	t_{su}	30.0	-	-	ns	
Data Input Hold Time	t_H	0.0	-	-	ns	

SPI3

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL=30pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	t_{CLK}/2-13	-	-	ns	
Chip Select Hold Time	t_{AG}	t_{CLK}-13	-	-	ns	
SCK Cycle	t_{CLK}	153.8	-	-	ns	
SCK Pulse Width-High	t_{CLKWL}	69.23	-	-	ns	
SCK Pulse Width-Low	t_{CLKWL}	69.23	-	-	ns	
Data Output Delay Time	t_{OD}	-13.0		13.0	ns	
Data Input Setup Time	t_{su}	40.0	-	-	ns	
Data Input Hold Time	t_H	0	-	-	ns	

SPI4

(VDD_CORE=1.0V(HP), VSS_DIG=0V reference, CL=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	tclk/2-2			ns	
Chip Select Hold Time	t_{AG}	tclk-2			ns	
SCK Cycle	t_{CLK}	25.7			ns	Tx
		103			ns	Rx
SCK Pulse Width-High	t_{CLKWL}	10.256			ns	Tx
		41.2			ns	Rx
SCK Pulse Width-Low	t_{CLKWL}	10.256			ns	Tx
		41.2			ns	Rx
Data Output Delay Time	t_{OD}	-3		8	ns	
Data Input Setup Time	t_{su}	15			ns	
Data Input Hold Time	t_H	0			ns	

(VDD_CORE=0.7V(LP), VSS_DIG=0V reference, CL=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	tclk/2-10			ns	
Chip Select Hold Time	t_{AG}	tclk-10			ns	
SCK Cycle	t_{CLK}	103			ns	Tx
		133			ns	Rx
SCK Pulse Width-High	t_{CLKWL}	46.35			ns	Tx
		59.8			ns	Rx
SCK Pulse Width-Low	t_{CLKWL}	46.35			ns	Tx
		59.8			ns	Rx
Data Output Delay Time	t_{OD}	-3		20	ns	
Data Input Setup Time	t_{su}	22			ns	
Data Input Hold Time	t_H	0			ns	

SPI5

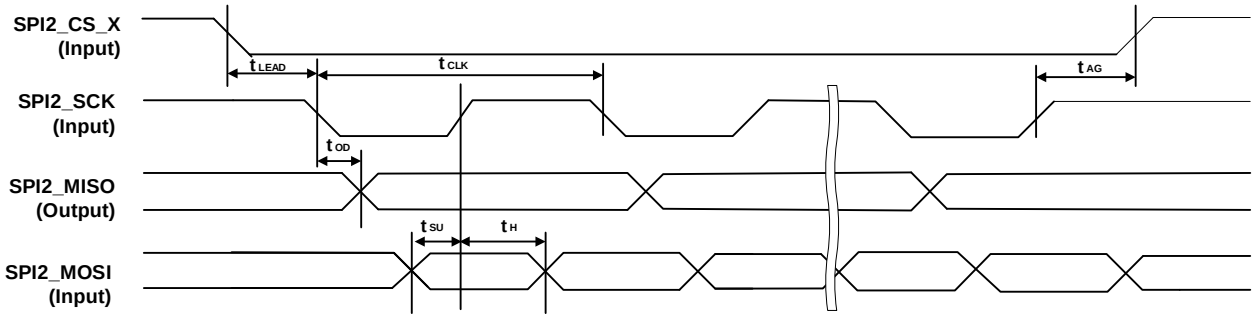
(VDD_CORE=1.0V(HP), VSS_DIG=0V reference, CL=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	tclk/2-5			ns	
Chip Select Hold Time	t_{AG}	tclk-5			ns	
SCK Cycle	t_{CLK}	76.9			ns	
SCK Pulse Width-High	t_{CLKWL}	34.6			ns	
SCK Pulse Width-Low	t_{CLKWL}	34.6			ns	
Data Output Delay Time	t_{OD}	-3		20	ns	
Data Input Setup Time	t_{su}	12			ns	
Data Input Hold Time	t_H	0			ns	

(VDD_CORE=0.7V(LP), VSS_DIG=0V reference, CL=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	tclk/2-13			ns	
Chip Select Hold Time	t_{AG}	tclk-13			ns	
SCK Cycle	t_{CLK}	154			ns	
SCK Pulse Width-High	t_{CLKWL}	70			ns	
SCK Pulse Width-Low	t_{CLKWL}	70			ns	
Data Output Delay Time	t_{OD}	-3		20	ns	
Data Input Setup Time	t_{su}	20			ns	
Data Input Hold Time	t_H	0			ns	

Slave Mode



SPI2

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL=30pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Chip Select Setup Time	t_{LEAD}	t_{LEAD_MIN}	-	-	ns	*1
Chip Select Hold Time	t_{AG}	t_{AG_MIN}	-	-	ns	*1
Chip Select High Time	t_{CS}	t_{CS_MIN}	-	-	ns	*1
SCK Cycle	t_{CLK}	t_{CLK_MIN}	-	-	ns	*1
Data Output Delay Time	t_{OD}	-	-	t_{OD_MAX}	ns	*1
Data Input Setup Time	t_{su}	13.0	-	-	ns	
Data Input Hold Time	t_H	0	-	-	ns	

*1) timings are relative to the internal clock frequency of the HOSTIFC block and they are listed below.

(Internal Clock Frequency and Timings)

Symbol	Internal Clock Frequency (MHz)					Notes
	RCOSC	XOSC		PLL		
		26/2	26	26*m/n	39‡ (26*6/4)†	
t_{LEAD_MIN}	462	423	192	230*n/m-38	115	
t_{AG_MIN}	924	847	385	460*n/m-76	231	
t_{CS_MIN}	462	423	192	230*n/m-38	115	
t_{CLK_MIN}	1000	923	461	460*n/m	307	
t_{OD_MAX}	276	257	141	115*n/m+26	103	

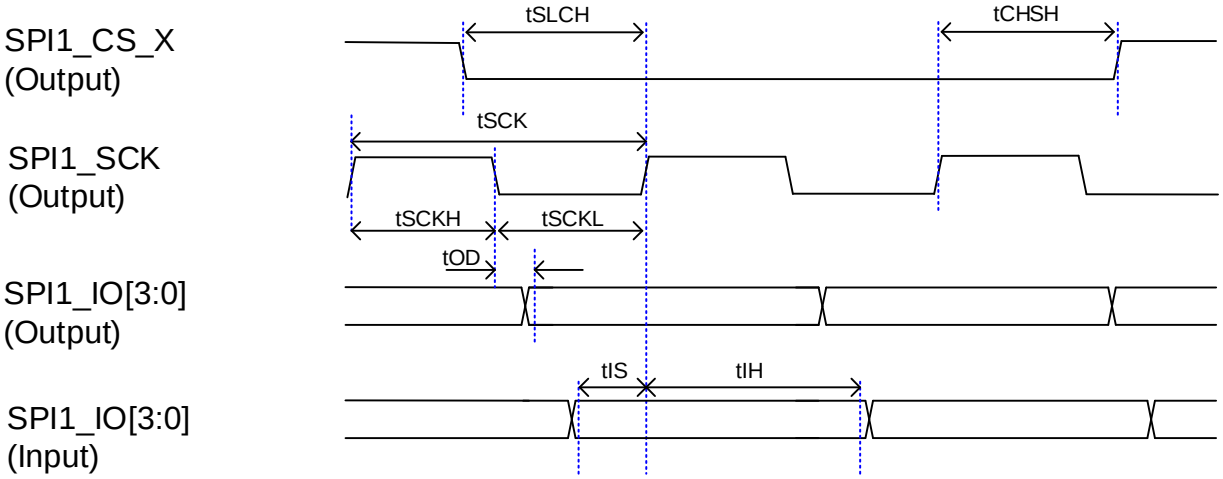
where m and n are positive integer.

† : HP (High Performance Only)

‡ : HOSTIFC internal maximum clock frequency

Quad SPI Flash Interface

Quad SPI Flash Interface (SPI1) is available.

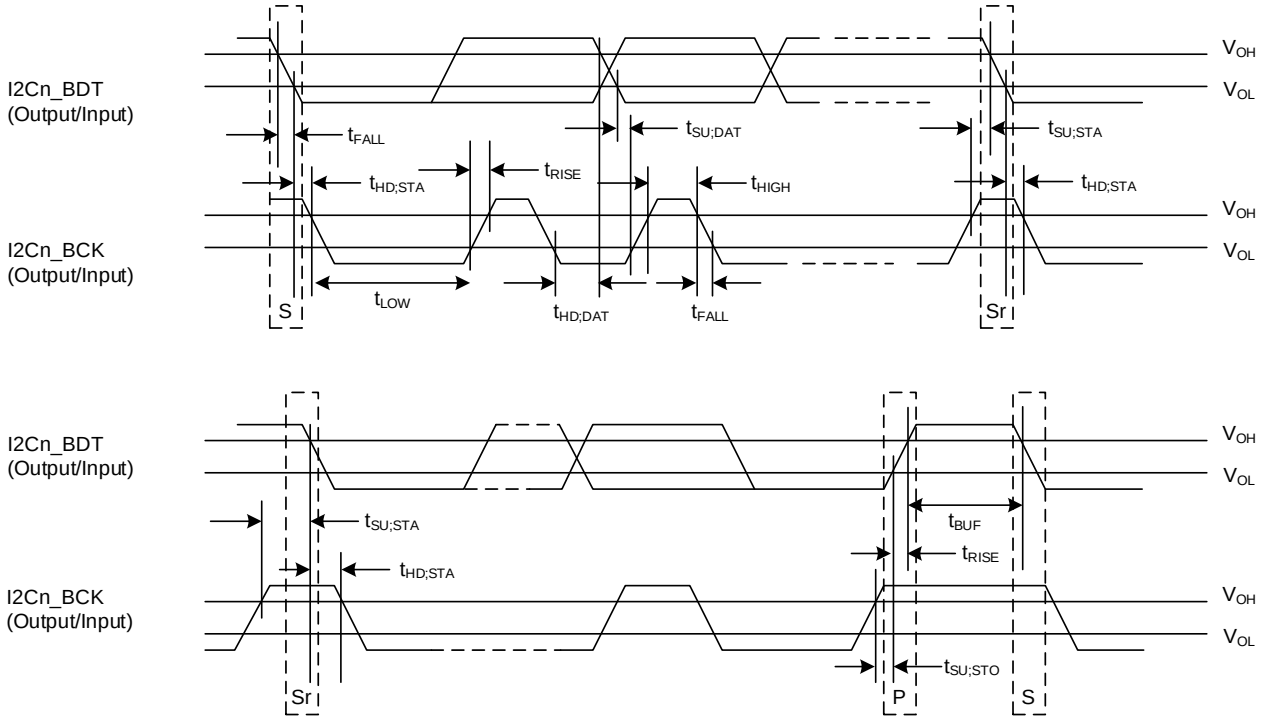


(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL=15pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
SPI1_SCK Period	tSCK	-	25.6	-	ns	39MHz
SPI1_SCK Duty Ratio	tSCKH / tSCK (tSCKL/tSCK)	40	50	60	%	-
SPI1_CS_X active setup time	tSLCH	7	-	-	ns	-
SPI1_CS_X active hold time	tCHSH	5	-	-	ns	-
SPI1_IO Output Delay Time	tOD	-10.36	-	12.86	ns	-
SPI1_IO Input Setup Time	tIS	0	-	-	ns	-
SPI1_IO Input Hold Time	tIH	15.36	-	-	ns	-

Inter-integrated circuit interface (I2C)

Up to four I2C bus interfaces can operate in multi-master mode (I2C0,I2C1,I2C2 and I2C4). They can support the standard (up to 100 kHz), and fast (up to 400 kHz) modes. And up to one I2C bus interface can operate slave mode (I2C3). They can support the standard (up to 100 kHz), fast (up to 400 kHz) and fast-mode plus (up to 1MHz).



I2C0

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL= refer to table)

Parameter	Symbol	Standard-Mode		Fast-Mode		-		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	-	-	kHz	
HOLD time (repeated) START condition	$T_{HD;STA}$	4.0	-	0.6	-	-	-	us	
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	-	-	us	
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	-	-	us	
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	-	-	us	
Data hold time; - For CBUS compatible masters - For I2C-bus devices	$t_{HD;DAT}$	 5.0 0	 - -	 - 0	 - -	-	-	us	
Data setup time	$t_{SU;DAT}$	250	-	100	-	-	-	ns	
Rise time of both SDA and SCL signals	t_{RISE}	-	1000	20	300	-	-	ns	
Fall time of both SDA and SCL signals	t_{FALL}	-	300	-	300	-	-	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	-	-	us	
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	-		us	

Capacitive load for each bus line	C_L		73		73		-	pF	4.7kohm PullUp

I2C1

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL= refer to table)

Parameter	Symbol	Standard-Mode		Fast-Mode		-		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	-	-	kHz	
HOLD time (repeated) START condition	$T_{HD;STA}$	4.0	-	0.6	-	-	-	us	
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	-	-	us	
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	-	-	us	
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	-	-	us	
Data hold time; - For CBUS compatible masters - For I2C-bus devices	$t_{HD;DAT}$	5.0 0	- -	- 0	- -	-	-	us	
Data setup time	$t_{SU;DAT}$	250	-	100	-	-	-	ns	
Rise time of both SDA and SCL signals	t_{RISE}	-	1000	20	300	-	-	ns	
Fall time of both SDA and SCL signals	t_{FALL}	-	300	-	300	-	-	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	-	-	us	
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	-	-	us	
Capacitive load for each bus line	C_L		73		73		-	pF	4.7kohm PullUp

I2C2

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL= refer to table)

Parameter	Symbol	Standard-Mode		Fast-Mode		-		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	-	-	kHz	
HOLD time (repeated) START condition	$T_{HD;STA}$	4.0	-	0.6	-	-	-	us	
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	-	-	us	
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	-	-	us	
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	-	-	us	
Data hold time; - For CBUS compatible masters - For I2C-bus devices	$t_{HD;DAT}$	5.0 0	- -	- 0	- -	-	-	us	
Data setup time	$t_{SU;DAT}$	250	-	100	-	-	-	ns	
Rise time of both SDA and SCL signals	t_{RISE}	-	1000	20	300	-	-	ns	

Fall time of both SDA and SCL signals	t_{FALL}	-	300	-	300	-	-	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	-	-	us	
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	-	-	us	
Capacitive load for each bus line	C_L		73		73	-	-	pF	4.7kohm PullUp

I2C3

(Fast-Mode Plus is only supported for I2C3_BCK/I2C3_BDT)

VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL= refer to table)

Parameter	Symbol	Standard-Mode		Fast-Mode		Fast-Mode Plus		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	0	1000	kHz	
HOLD time (repeated) START condition	$T_{HD;STA}$	4.0	-	0.6	-	0.26	-	us	
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	0.5		us	
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	0.26		us	
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	0.26		us	
Data hold time; - For CBUS compatible masters - For I2C-bus devices	$t_{HD;DAT}$	 5.0 0	 - -	 - 0	 - -	-	-	us	
Data setup time	$t_{SU;DAT}$	250	-	100	-	50	-	ns	
Rise time of both SDA and SCL signals	t_{RISE}	-	1000	20	300	-	120	ns	
Fall time of both SDA and SCL signals	t_{FALL}	-	300	-	300	6.5	120	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	0.26	-	us	
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	0.5		us	
Capacitive load for each bus line	C_L		73		73		29	pF	4.7kohm PullUp

I2C4

(VDD_CORE=0.7V(LP)/1.0V(HP), VSS_DIG=0V reference, CL= refer to table)

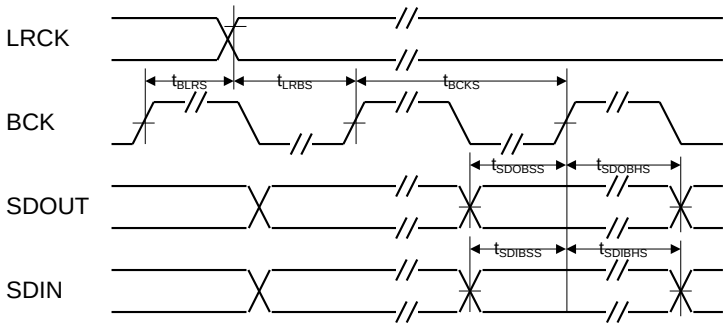
Parameter	Symbol	Standard-Mode		Fast-Mode		-		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
SCL clock frequency	f_{SCL}	0	100	0	400	-	-	kHz	
HOLD time (repeated) START condition	$T_{HD;STA}$	4.0	-	0.6	-	-	-	us	
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	-	-	us	
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	-	-	us	
Setup time for a repeated START condition	$t_{SU;STA}$	4.7	-	0.6	-	-	-	us	
Data hold time; - For CBUS compatible masters - For I2C-bus devices	$t_{HD;DAT}$	 5.0 0	 - -	 - 0	 - -	-	-	us	
Data setup time	$t_{SU;DAT}$	250	-	100	-	-	-	ns	
Rise time of both SDA and SCL signals	t_{RISE}	-	1000	20	300	-	-	ns	
Fall time of both SDA and SCL signals	t_{FALL}	-	300	-	300	-	-	ns	
Setup time for STOP condition	$t_{SU;STO}$	4.0	-	0.6	-	-	-	us	
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	-	-	us	
Capacitive load for each bus line	C_L		73		73	-	-	pF	4.7kohm PullUp

Universal Asynchronous Receiver Transmitter (UART)

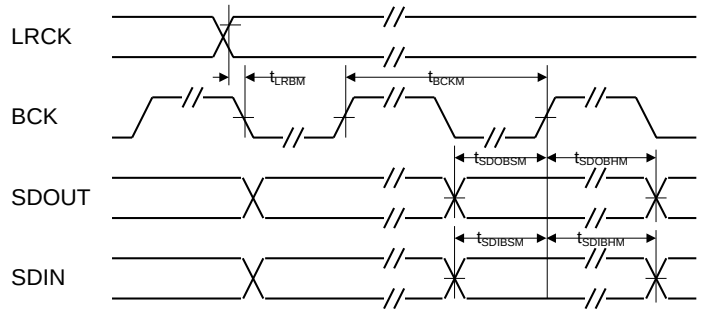
The device supports up to three universal asynchronous receiver transmitters (UART0, UART1 and UART2). UART0 and UART2 provide hardware management of the CTS and RTS signals (support flow control) .

Inter-integrated sound (I2S)

Up to two I2S interfaces (I2S0 and I2S1) are available.



Serial Digital Interface Timing (Slave mode)



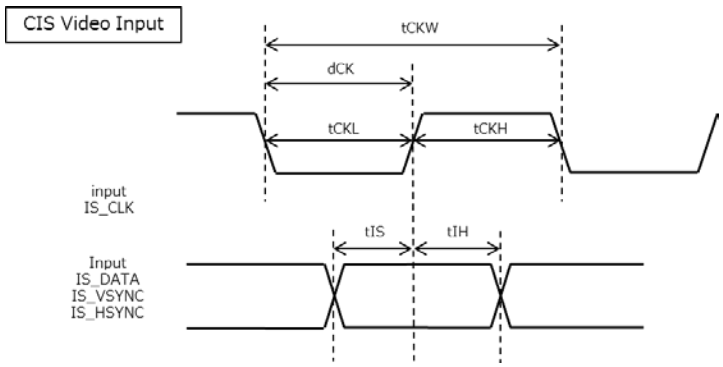
Serial Digital Interface Timing (Master mode)

Parameters	Symbol	Min	Typ	Max	Condition	Units
MCLK frequency	F_{MCLK2}	-	24.576	-		MHz
MCLK duty cycle	DC_{MCLK}		50			%
Input sample rate (LRCK)	fs'	8	-	216		kHz
LRCK duty cycle	DC_{LRCK}	45	-	55		%
BCK duty cycle	DC_{BCK}	45	-	55		%
Slave mode						
BCK Frequency	$1/t_{BCKS}$	-	-	64•fs'	High Performance Mode	Hz
		-	-	32•fs'	Low Power Mode	
LRCK edge to BCK "↑"	t_{LRBS}	20	-	-		ns
BCK "↑" to LRCK edge	t_{BLRS}	20	-	-		ns
SDOUT hold time to BCK "↑"	t_{SDOBHS}	20	-	-		ns
SDOUT setup time to BCK "↑"	t_{SDOBSS}	20	-	-		ns
SDIN hold time to BCK "↑"	t_{SDIBHS}	20	-	-		ns
SDIN setup time to BCK "↑"	t_{SDIBSS}	20	-	-		ns
Master mode						
BCK Frequency	$1/t_{BCKM}$	-	64•fs	-	High Performance Mode	Hz
		-	32•fs	-	Low Power Mode	
LRCK edge to BCK "↑"	t_{LRBM}	-2	-	+2		ns
SDOUT hold time to BCK "↑"	t_{SDOBHM}	20	-	-		ns
SDOUT setup time to BCK "↑"	t_{SDOBSM}	20	-	-		ns
SDIN hold time to BCK "↑"	t_{SDIBHM}	20	-	-		ns
SDIN setup time to BCK "↑"	t_{SDIBSM}	20	-	-		ns

Unique Audio Data Format (Pulse Density Modulation) between CXD5602GG and CXD5247GF

The audio master clock MCLK clock frequency is 24.567MHz (Typ.). The serialized audio signals PDM_CLK, PDM_IN and PDM_OUT are specified by MCLK.

Image Sensor Interface



Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Input CLK Period	dCK	-	-	-	ns	54MHz
Data input setup time	tIS	4.5	-	-	ns	-
Data input hold time	tiH	4.5	-	-	ns	-

SD Host Interface

A SD host interface supports SD Memory Card Protocol version 3.0 in two different databus modes: 1-bit (default) and 4-bit.

eMMC Interface

An eMMC interface supports eMMC 4.41 Protocol compatible in two different databus modes: 1-bit (default) and 4-bit.

Universal serial bus (USB) Device

An USB Device is compliant with USB 2.0 Specification High-speed up to 480 Mbps.

The main features are:

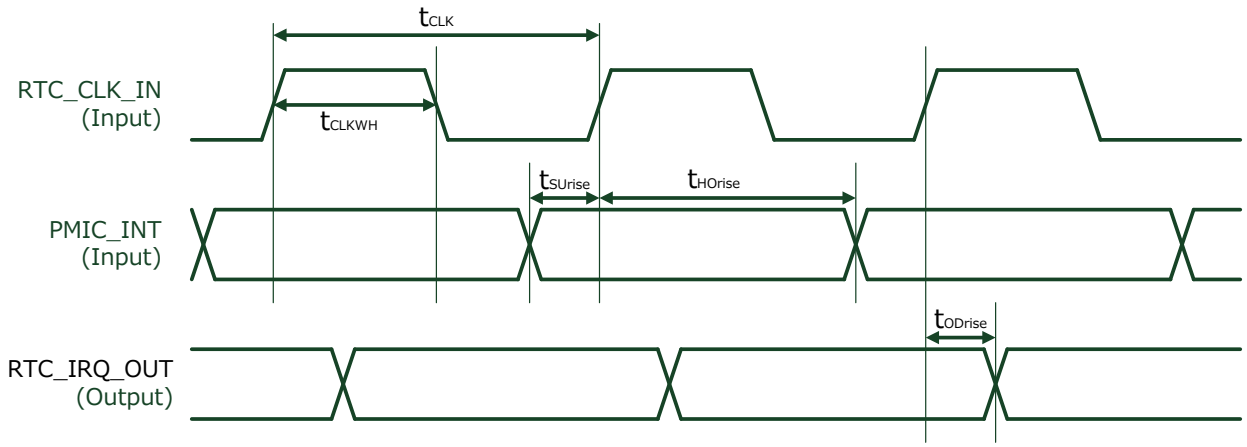
MSC, MTP, CDC, PTP, ACM, and HID class

Multi-function: Interface: #0/#1/#2

RTC Signals

RTC Signals are RTC_CLK_IN, PMIC_INT and RTC_IRQ_OUT. These signals are between CXD5602GG and CXD5247GF.

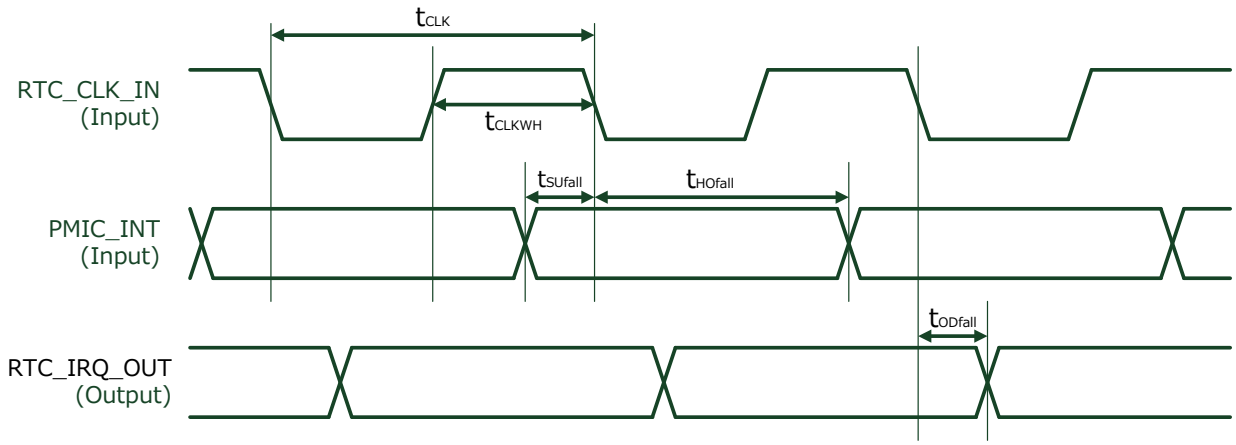
Rise Edge Detection Mode



(VDDC=0.7V(LP)/1.0V(HP), Vss=0V reference, CL=25pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
RTC_CLK_IN Clock Cycle	t_{CLK}	-	30.51	-	us	RTC_CLK_IN = 32.768KHz
RTC_CLK_IN Pulse Width-High	t_{CLKWH}	3.051	-	27.459	us	
Data Input Setup Time	t_{SUrise}	20.0	-	-	ns	
Data Input Hold Time	t_{HOrise}	2.0	-	-	ns	
Data Output Delay Time	t_{ODrise}	2.0	-	100.0	ns	

Fall Edge Detection Mode



(VDDC=0.7V(LP)/1.0V(HP), Vss=0V reference, CL=25pF)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
RTC_CLK_IN Clock Cycle	t_{CLK}	-	30.51	-	us	RTC_CLK_IN = 32.768KHz
RTC_CLK_IN Pulse Width-High	t_{CLKWH}	3.051	-	27.459	us	
Data Input Setup Time	t_{SUfall}	20.0	-	-	ns	
Data Input Hold Time	t_{HOfall}	2.0	-	-	ns	
Data Output Delay Time	t_{ODfall}	2.0	-	100.0	ns	

ADC Analog Input Interface

HPADC analog input interface. (SEN_AIN0, SEN_AIN1)[i]

Parameter	Min.	Typ.	Max.	Units	Notes
Conversion Rate		2		MS/s	
Input signal Bandwidth		32		kHz	LPF through
Input signal full scale		1.6 0.8 0.4 0.2 0.16		Vpp	LPF -6dB LPF 0dB LPF +6dB LPF +12dB LPF +14dB
Input signal range			1.44 0.72 0.36 0.18 0.144	Vpp	LPF gain -6dB LPF gain 0dB LPF gain +6dB LPF gain +12dB LPF gain +14dB
Resolution			10	bits	
DNL	-1		2	LSB	
INL	-4		4	LSB	
SNR	53.7 52.1			dB dB	0.72 Vpp input, LPF gain 0dB(including LPF) 1.2 Vpp input, LPF gain -6dB(including LPF)
SNDR	28.6 44.5			dB dB	0.72 Vpp input, LPF gain 0dB(including LPF) 1.2 Vpp input, LPF gain -6dB(including LPF)

LPADC analog input interface. (SEN_AIN2, SEN_AIN3, SEN_AIN4, SEN_AIN5)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Conversion Rate	fclk		32 256		kS/s S/s	1ch 4ch
Input signal range	FS		VDDA_ANA_M		Vpp	
Resolution				10	bits	
ENOB		8.4			-	
DNL		-1		1.7	LSB	
INL		-4		4	LSB	
SNR	SNR	51.7			dB	
SNDR	SNDR	51.4			dB	

[i] Connection to HPADC should be AC coupling.

Serial wire debug (SWD)

The CXD5602GG provides the ARM SWD interface.

Notes on Handling

- The power supply and GND patterns have a large effect on undesired radiation on the board and interference to analog circuits, etc. Please refer to application notes of the CXD5602GG.
- Do not use this IC under conditions other than the recommended operating conditions.
- Absolute maximum rating values should not be exceeded even momentarily. It may damage the device, leading to eventual breakdown.
- This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.
- Since this IC utilizes a MOS structure, it may latch up due to excessive noise or power surge greater than the maximum rating of the I/O pins, interface with two power supplies of another circuit, or the order in which power is supplied to circuits. Make a thorough study of measures against the possibility of latch up before use.
- Keep recommended power-on and power-off sequences for embedded power on reset.
- Be sure to make a thorough evaluation of any items not listed in this data sheet.

Pin Configuration

I2C3, SPI2 and UART0 interfaces multiplexed with each other, so one interface is available.

STRAP PIN: SYSTEM0, SYSTEM1

SYSTEM1	SYSTEM0	Host Interface
0	0	I2C3
0	1	UART0
1	0	SPI2
1	1	reserved

Pin Description

Pin Number	Name (functions)	Type	I/O	IO Power Supply	Reset State	Alternate functions
C7	TEST0	Digital	I	VDD_IO_DIG	Hi-Z	
D7	SYSTEM0	Digital	I	VDD_IO_DIG	Hi-Z	SWDCLK
D8	SYSTEM1	Digital	I/O	VDD_IO_DIG	Hi-Z	SWDIO
B8	BOOT_MODE	Digital	I	VDD_IO_DIG	PullDown	
C8	BOOT_REC	Digital	I	VDD_IO_DIG	PullDown	
E1	XOSC_IN	Analog	I/O	VDDA_SENS	-	XOSC_IN
F1	XOSC_OUT	Analog	I/O		-	XOSC_OUT
A8	RTC_CLK_IN	Digital	I	VDD_IO_DIG	Hi-Z	RTC_CLK_IN
B9	RST_X	Digital	I	VDD_IO_DIG	Hi-Z	RST_X
B10	P10_00	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C4_BCK
B11	P10_01	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C4_BDT
C10	P11_00	Digital	I/O	VDD_IO_DIG	Hi-Z	PMIC_INT,RTC_IRQ_OUT
D10	P12_00	Digital	I/O	VDD_IO_DIG	Hi-Z	RTC_IRQ_OUT
A11	P13_00	Digital	I/O	VDD_IO_DIG	Hi-Z	AP_CLK,PMU_WDT
B12	P14_00	Digital	I/O	VDD_IO_DIG	Hi-Z	GNSS_1PPS_OUT,CPU_WDT
D13	P16_00	Digital	I/O	VDD_IO_DIG	Hi-Z	UART1_TXD,SPI0_CS_X
C14	P16_01	Digital	I/O	VDD_IO_DIG	Hi-Z	UART1_RXD,SPI0_SCK
D12	P17_00	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C2_BCK,SPI0_MOSI
D11	P17_01	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C2_BDT,SPI0_MISO
A13	P18_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_CS_X,SPI0_CS_X
A14	P18_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_SCK,SPI0_SCK
B13	P18_02	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_IO0,SPI0_MOSI
C13	P18_03	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_IO1,SPI0_MISO
C12	P19_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_IO2
C11	P19_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI1_IO3
A1	GNSS_RF_IN	Analog	I	VSSA_SENS	-	
C1	DCXO_IB_OUT	Analog	O	VDDA_SENS	-	
A6	P00_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI2_CS_X,UART0_TXD,I2C3_BCK
B7	P00_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI2_SCK,UART0_RXD,I2C3_BDT
B6	P01_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI2_MOSI,UART0_CTS,
C6	P01_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI2_MISO,UART0_RTS,
D6	P02_00	Digital	I/O	VDD_IO_DIG	Hi-Z	HIF_IRQ_OUT,GNSS_1PPS_OUT
E6	P03_00	Digital	I/O	VDD_IO_DIG	Hi-Z	GPS_EXTLD
J1	SEN_AIN0	Analog	I	VDDA_SENS	-	

Pin Number	Name (functions)	Type	I/O	IO Power Supply	Reset State	Alternate functions
K1	SEN_AIN1	Analog	I	VDDA_SENS	-	
J2	SEN_AIN2	Analog	I		-	
H2	SEN_AIN3	Analog	I		-	
K2	SEN_AIN4	Analog	I		-	
L1	SEN_AIN5	Analog	I		-	
P5	P1e_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SEN_IRQ_IN
N5	P1f_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_CS0_X
M6	P1g_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_CS1_X
M5	P1h_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_CS2_X
N4	P1i_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_SCK
M4	P1i_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_MOSI
L4	P1i_02	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI3_MISO
P4	P1j_00	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C0_BCK
N3	P1j_01	Digital	I/O	VDD_IO_DIG	Hi-Z	I2C0_BDT
L5	P1k_00	Digital	I/O	VDD_IO_DIG	Hi-Z	PWM0
L6	P1k_01	Digital	I/O	VDD_IO_DIG	Hi-Z	PWM1
L7	P1l_00	Digital	I/O	VDD_IO_DIG	Hi-Z	PWM2,I2C1_BCK
L8	P1l_01	Digital	I/O	VDD_IO_DIG	Hi-Z	PWM3,I2C1_BDT
K14	P1m_00	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_CLK
J14	P1m_01	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_VSYNC
J13	P1m_02	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_HSYNC
K13	P1m_03	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA0
K12	P1m_04	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA1
K11	P1m_05	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA2
K10	P1m_06	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA3
L14	P1m_07	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA4
L13	P1m_08	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA5
L12	P1m_09	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA6
L11	P1m_10	Digital	I/O	VDD_IO_DIG	Hi-Z	IS_DATA7
M14	P1n_00	Digital	I/O	VDD_IO_DIG	Hi-Z	UART2_TXD
M13	P1n_01	Digital	I/O	VDD_IO_DIG	Hi-Z	UART2_RXD
M12	P1n_02	Digital	I/O	VDD_IO_DIG	Hi-Z	UART2_CTS
M11	P1n_03	Digital	I/O	VDD_IO_DIG	Hi-Z	UART2_RTS
N14	P1o_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI4_CS_X
P14	P1o_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI4_SCK
N13	P1o_02	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI4_MOSI

Pin Number	Name (functions)	Type	I/O	IO Power Supply	Reset State	Alternate functions
N12	P1o_03	Digital	I/O	VDD_IO_DIG	Hi-Z	SPI4_MISO
P6	EMMC_CLK	Digital	I/O	VDD_IO_DIG	0	P1p_00, SPI5_CS_XSPI5_SCK
N6	P1p_01	Digital	I/O	VDD_IO_DIG	Hi-Z	EMMC_CMD, SPI5_CS_XSPI5_SCK
N7	P1p_02	Digital	I/O	VDD_IO_DIG	Hi-Z	EMMC_DATA0,SPI5_MOSI
N8	P1p_03	Digital	I/O	VDD_IO_DIG	Hi-Z	EMMC_DATA1,SPI5_MISO
M7	P1q_00	Digital	I/O	VDD_IO_DIG	Hi-Z	EMMC_DATA2
M8	P1q_01	Digital	I/O	VDD_IO_DIG	Hi-Z	EMMC_DATA3
P8	P1r_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_CLK, SPI5_SCK SPI5_CS_X
P9	P1r_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_CMD,SPI5_SCK SPI5_CS_X
P10	P1r_02	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DATA0,SPI5_MOSI
N9	P1r_03	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DATA1,SPI5_MISO
M9	P1r_04	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DATA2
L9	P1r_05	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DATA3
P11	P1s_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_CD
P12	P1s_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_WP
N10	P1t_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_CMDDIR
M10	P1t_01	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DIR0
L10	P1t_02	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_DIR1_3
N11	P1u_00	Digital	I/O	VDD_IO_DIG	Hi-Z	SDIO_CLKI
E14	P1v_00	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S0_BCK
E13	P1v_01	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S0_LRCK
E12	P1v_02	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S0_DATA_IN
E11	P1v_03	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S0_DATA_OUT
F14	P1w_00	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S1_BCK
F13	P1w_01	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S1_LRCK
F12	P1w_02	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S1_DATA_IN
F11	P1w_03	Digital	I/O	VDD_IO_DIG	Hi-Z	I2S1_DATA_OUT
H14	P1x_00	Digital	I/O	VDD_IO_DIG	Hi-Z	MCLK
H13	P1y_00	Digital	I/O	VDD_IO_DIG	Hi-Z	PDM_CLK
H11	P1y_01	Digital	I/O	VDD_IO_DIG	Hi-Z	PDM_IN
H12	P1y_02	Digital	I/O	VDD_IO_DIG	Hi-Z	PDM_OUT
P1	USB_DP	Analog	I/O	VDDA_USB33	-	
N1	USB_DM	Analog	I/O	VDDA_USB33	-	
M1	USB_TXRTUNE	Analog	I/O	VDDA_USB18	-	
P3	P1z_00	Digital	I/O	VDD_IO_DIG	Hi-Z	USB_VBUSINT
E9	SWOCLK	Digital	O	VDD_IO_DIG	Hi-Z	

Pin Number	Name (functions)	Type	I/O	IO Power Supply	Reset State	Alternate functions
C9	SWO	Digital	O	VDD_IO_DIG	Hi-Z	

Power Pins

Pin Number	Name	Power Group	Description
J6,K6,K7, H6	VDD_CORE	Vdd	
G9,H9,J9, F9	VDD_IO_DIG	Vdd	
A3	VDDA_IO_ANA	Vdd	
F2	VDDA_IO_SENS	Vdd	
A2	VDDA_LNA	Vdd	
C3	VDDA_LO	Vdd	
B4	VDDA_ANA_M	Vdd	
E3	VDDA_SYSPLL_M	Vdd	
G1	VDDA_XOSC	Vdd	
F3	VDDA_LPADC	Vdd	
G3	VDDA_HPADC_M	Vdd	
M3	VDDA_USB33	Vdd	
M2	VDDA_USB18_M	Vdd	
L3	VDDA_USB10_M	Vdd	
A7,A9,A10,A12,B14,D14,E5,E7,E8, E10,F6,F10,G6,G10,G11,G12, G13,G14,H5,H10,J5,J10,J11,J12,K5,K8 ,K9,P7P13,D9	VSS_DIG	Vss	
A4, A5,B5,C5,D5,D4,C4,D3	VSSA_AIN	Vss	
G2,H1	VSSA_SENS	Vss	
-	VSSA_IO_M	Vss	
B1,B2,C2	VSSA_LNA	Vss	
D2	VSSA_LO	Vss	
B3	VSSA_ANA_M	Vss	
E2	VSSA_SYSPLL_M	Vss	
D1	VSSA_XOSC	Vss	
F4,K3,L2,G5,F5,H4,J3,H3	VSSA_LPADC	Vss	
G4	VSSA_HPADC_M	Vss	
N2,P2	VSSA_USB_M	Vss	

Ball Map

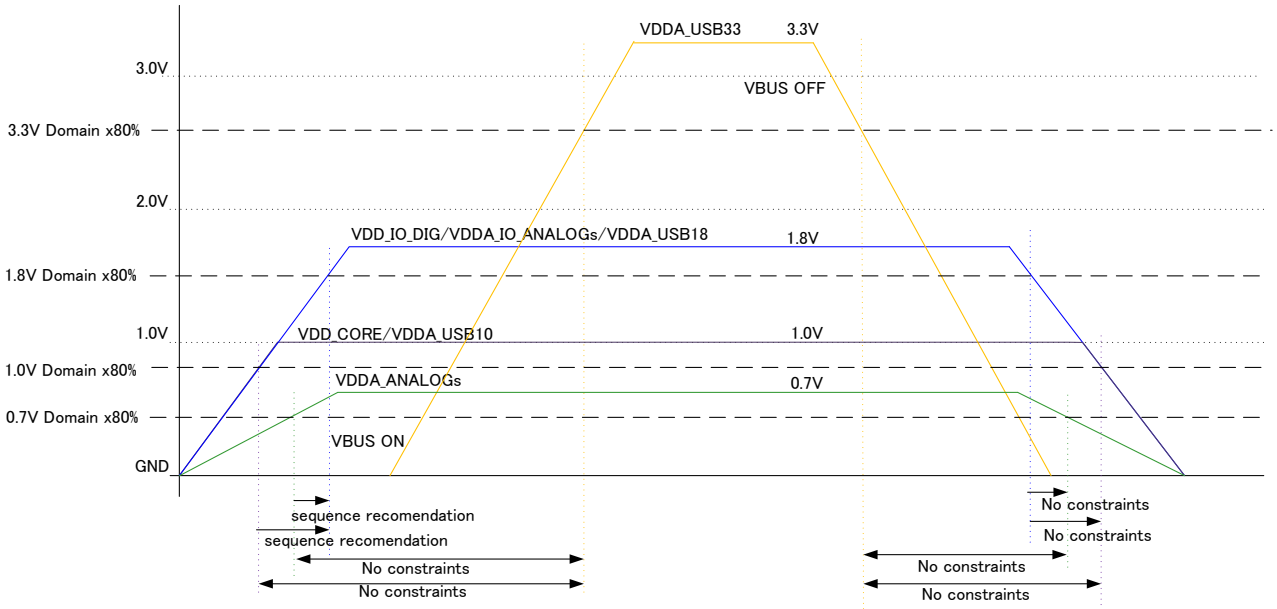
MFC VFBGA 185pin.

Bottom View

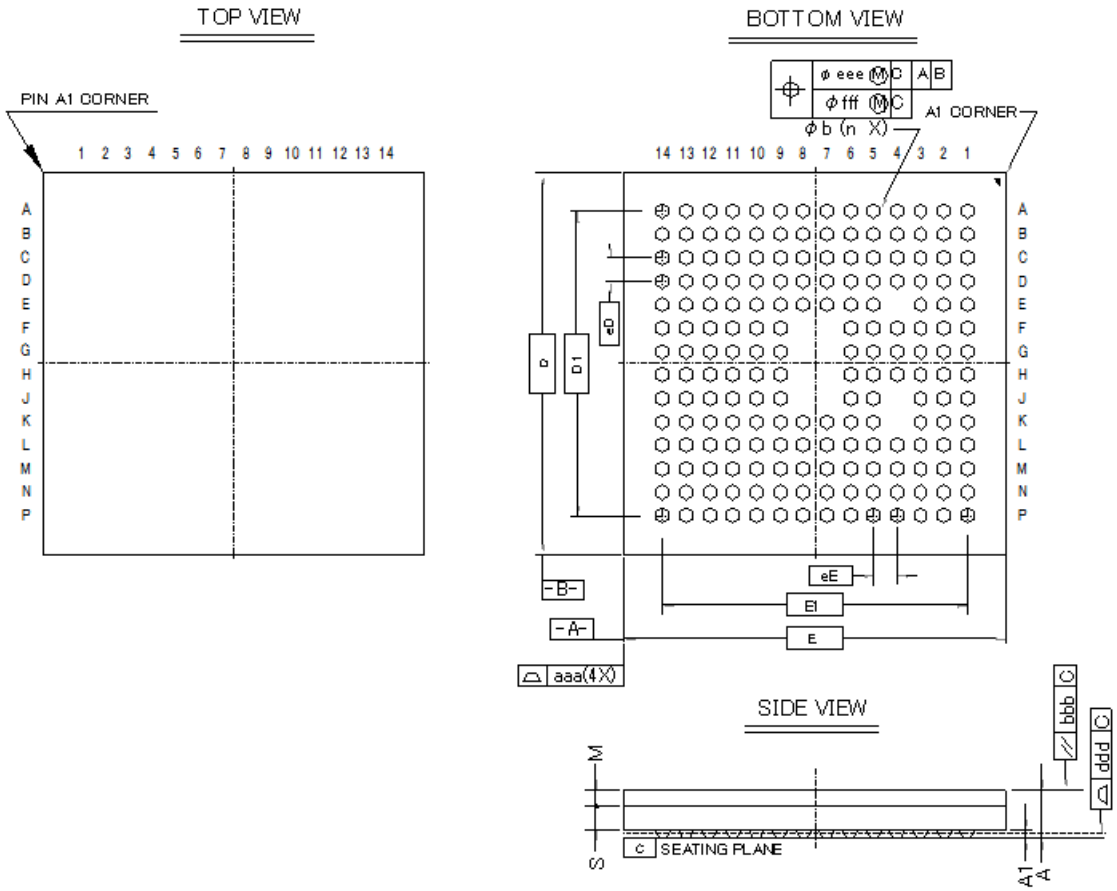
A	B	C	D	E	F	G	H	J	K	L	M	N	P	
GNSS_RF_IN	VSSA_LNA	DCXO_IB_OUT	VSSA_XOSC	XOSC_IN	XOSC_OUT	VDDA_XOSC	VSSA_SENS	SEN_AIN0	SEN_AIN1	SEN_AIN5	USB_TXRTUNE	USB_DM	USB_DP	1
VDDA_LNA	VSSA_LNA	VSSA_LNA	VSSA_LO	VSSA_SYSPLL_M	VDDA_IO_SENS	VSSA_SENS	SEN_AIN3	SEN_AIN2	SEN_AIN4	VSSA_LPADC	VDDA_USB18_M	VSSA_USB_M	VSSA_USB_M	2
VDDA_IO_ANA	VSSA_ANA_M	VDDA_LO	VSSA_AIN	VDDA_SYSPLL_M	VDDA_LPADC	VDDA_HPADC_M	VSSA_LPADC	VSSA_LPADC	VSSA_LPADC	VDDA_USB10_M	VDDA_USB33	N3	P3	3
VSSA_AIN	VDDA_ANA_M	VSSA_AIN	VSSA_AIN	NC	VSSA_LPADC	VSSA_HPADC_M	VSSA_LPADC	NC	NC	L4	M4	N4	P4	4
VSSA_AIN	VSSA_AIN	VSSA_AIN	VSSA_AIN	VSS_DIG	VSSA_LPADC	VSSA_LPADC	VSS_DIG	VSS_DIG	VSS_DIG	L5	M5	N5	P5	5
A6	B6	C6	D6	E6	VSS_DIG	VSS_DIG	VDD_CORE	VDD_CORE	VDD_CORE	L6	M6	N6	P6	6
VSS_DIG	B7	C7	D7	VSS_DIG	NC	NC	NC	NC	VDD_CORE	L7	M7	N7	VSS_DIG	7
A8	B8	C8	D8	VSS_DIG	NC	NC	NC	NC	VSS_DIG	L8	M8	N8	P8	8
VSS_DIG	B9	C9	VSS_DIG	E9	VDD_IO_DIG	VDD_IO_DIG	VDD_IO_DIG	VDD_IO_DIG	VSS_DIG	L9	M9	N9	P9	9
VSS_DIG	B10	C10	D10	VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	VSS_DIG	K10	L10	M10	N10	P10	10
A11	B11	C11	D11	E11	F11	VSS_DIG	H11	VSS_DIG	K11	L11	M11	N11	P11	11
VSS_DIG	B12	C12	D12	E12	F12	VSS_DIG	H12	VSS_DIG	K12	L12	M12	N12	P12	12
A13	B13	C13	D13	E13	F13	VSS_DIG	H13	J13	K13	L13	M13	N13	VSS_DIG	13
A14	VSS_DIG	C14	VSS_DIG	E14	F14	VSS_DIG	H14	J14	K14	L14	M14	N14	P14	14

Power On/Off sequence

To avoid occurring reliability problem and loading external power supply system, turning on the I/O power supply(1.8V Domain) and then turning on the internal power supply(1.0/0.7V Domain) is recommended for power on. In addition, shutting down the internal power supply (1.0/0.7V Domain) and then shutting down the I/O power supply (1.8V Domain) in the reverse order of turning on is recommended for power off.



CXD5602GG: MFC VFBGA 185pin

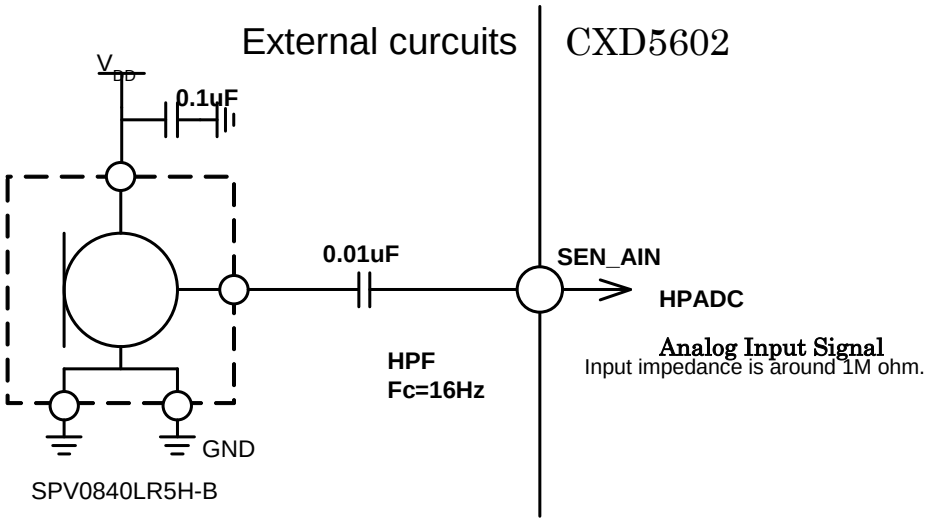


		Symbol	Common Dimensions
Package :			MFC VFBGA
Body Size:	X	E	6.500
	Y	D	6.500
Ball Pitch :	X	eE	0.400
	Y	eD	0.400
Total Thickness :		A	1.000 Max.
Mold Thickness :		M	0.280 Ref.
Substrate Thickness :		s	0.400 Ref.
Ball Diameter :			0.250
Stand Off :		A1	0.110 ~ 0.210
Ball Width :		b	0.200 ~ 0.300
Package Edge Tolerance :		aaa	0.100
Mold Flatness :		bbb	0.100
Coplanarity:		ddd	0.080
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.050
Ball Count :		n	185
Edge Ball Center to Center :	X	E1	5.200
	Y	D1	5.200

Application Circuits.

Analog MIC. Fc is calculated using following formula.

Fc=1/(2*pi*Ccoupling[0.01uF]*HPADC input impedance[1Mohm]



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Furthermore, usage of the Products for military purposes is strictly prohibited at all times.

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